

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
14.5			2009-06-12

K84 MLB SCHEMATIC
PVT 06/12/2009

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52	66	AUDIO: SPEAKER AMP	A0010	06/09/2009
53	67	AUDIO: JACK	A0010	06/09/2009
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57	72	5V/3.3V SUPPLY		
58	73	1.5V/0.75V DDR3 SUPPLY		
59	74	IMVP6 CPU VCore Regulator	E24_HL8L	03/03/2009
60	75	MCP CORE REGULATOR	E24_HL8L	02/15/2009
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70	100	CPU/FSB Constraints	E24_HL8L	04/04/2009

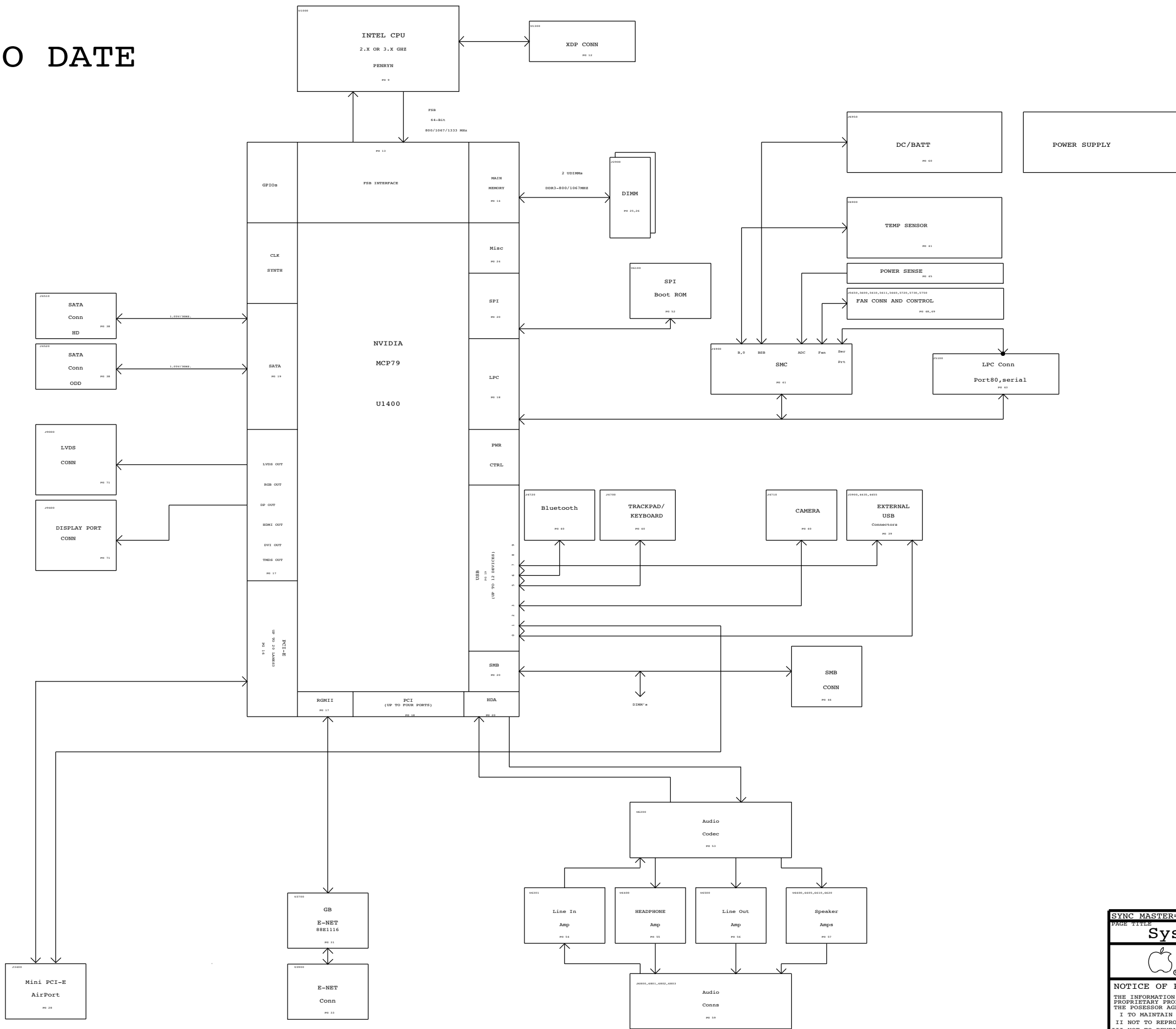
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72	102	MCP Constraints 1	K24_HLS	03/30/2009
73	103	MCP Constraints 2	K24_HLS	04/06/2009
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7982	1	SCHEM,MLB,K84	SCH	CRITICAL	
820-2567	1	PCBF,MLB,K84	PCB		

DRAWING TITLE		DRAWING NUMBER		SIZE
SCHEM, MLB, K84		051-7982		D
 Apple Inc.		REVISION		
		14.5.0		
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SYNC MASTER=K24 MLB

SYNC DATE=01/19/2009

System Block Diagram

 Apple Inc.

DRAWING NUMBER
051-7982

REVISION
14.5.0

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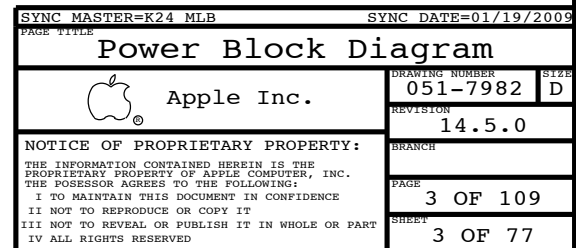
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0035	PCBA,MLB,FOX DDR CONN,K84	K84_COMMON,CPU_2_0GHZ,FOX_DDR_CONN,EEF_8CG
639-0254	PCBA,MLB,HLX DDR CONN,K84	K84_COMMON,CPU_2_0GHZ,HLX_DDR_CONN,EEF_A36
085-0748	K84 MLB DEVELOPMENT BOM	K84_DEVEL_ENG

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCR,28MM X 6 MM	[EEE]8CG	CRITICAL	EEE_8CG
826-4393	1	LBL,P/N LABEL,PCR,28MM X 6 MM	[EEE]A36	CRITICAL	EEE_A36

BOM Groups

BOM GROUP	BOM OPTIONS
K84_COMMON	COMMON,ALTERNATE,K84_MCP,K84_MISC,K84_DEBUG_ENG,K84_PROGPARTS
K84_MCP	MCP_B03,BOOT_MODE_USER,MCPSEQ_SMC
K84_MISC	QWIRE_FU_PD_ESD,MKEY,L50_NO,MKEY_LOAD_DET,HEM_SENSE,1P05_HIGH_SIDE_SENSE,MCP_T_DIODE_SENSOR,MCP5MC_DIGITEMP_YES
K84_PROGPARTS	BOOTROM_PROG,SMC_PROG,WELLSPRING_PROG
K84_DEBUG_ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K84_DEBUG_PVT	DEVEL_BOM,SMC_DEBUG_YES,XDP,NO_VREFMRGN
K84_DEBUG_PROD	SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN
K84_DEVEL_ENG	DEBUG_ADC,XDP_CONN,LPCPLUS,VREFMRGN
K84_DEVEL_PVT	LPCPLUS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33753704	1	DOC,SLD23,PWG,2.7K,25W,1066,80,3H,BGA	U1000	CRITICAL	CPU_2_OGH2
33880710	1	IC,MCIP,MCP79,35X35MM,BGA1437,B03	U1400	CRITICAL	MCP_B03
51680706	1	CONN,204P,SOD108,SOCKET,DDR3,8AM,BGA	J3200	CRITICAL	FOX_DDR_CONN
516-0201	1	CONN,204P,SOD108,P=0.6MM	J3100	CRITICAL	FOX_DDR_CONN
51680790	1	CONN,204P,SOD108,SOCKET,DDR3,8AM,NON/SC	J3200	CRITICAL	HLX_DDR_CONN
516-0213	1	CONN,204P,SOD108,P=0.6MM,RF	J3100	CRITICAL	HLX_DDR_CONN
452-1708	4	SCR,M1.6X0.35X6.0,D4,B0.3,HLX,M97	SCREW1,SCREW2,SCREW3,SCREW4	CRITICAL	

DEVELOPMENT BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0748	1	K84 HLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM

Programmable Parts

33880563	1	IC,SMC,RSE/2117,PA99M,TLP,RF	U4900	CRITICAL	SMC_BLANK
34182485	1	IC,SMC,K84	U4900	CRITICAL	SMC_PROG
33580610	1	IC,FLASH,EPT,32MBIT,3.3V,66MHz,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
34182487	1	IC,PRGRM,EPT BOOTROM,UNLOCK,K84	U6100	CRITICAL	BOOTROM_PROG
33782983	1	IC,F80C+ W/ USB,56 PIN,HLP,CYC824794	U5701	CRITICAL	WELLSPRING_BLANK
34182491	1	IC,WELLSPRING CONTROLLER,K84	U5701	CRITICAL	WELLSPRING_PROG

LOCKED BOOTROM APN IS 341S2488

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15280693	15280778		ALL	DALE/VISSAY, NAGLAYERS AS ALTERNATE
15280796	15280685		ALL	CYWEC AS ALTERNATE
15780058	15780055		ALL	DELTA AS ALTERNATE
13880603	13880602		ALL	MURATA AS ALTERNATE
12880093	12880218		ALL	SENET AS ALTERNATE
15280874	15280516		ALL	NAGLAYERS AS ALTERNATE
15280847	15280586		ALL	NAGLAYERS AS ALTERNATE
10480018	10480023		ALL	DALE/VISSAY AS ALTERNATE
514-0690	514-0691		ALL	PLASTIC PART AS ALTERNATE
514-0688	514-0689		ALL	PLASTIC PART AS ALTERNATE
35382718	35382310		ALL	NEW INTERSIL PART AS ALTERNATE
13880661	13880540		ALL	LOW NOISE MURATA AS ALTERNATE

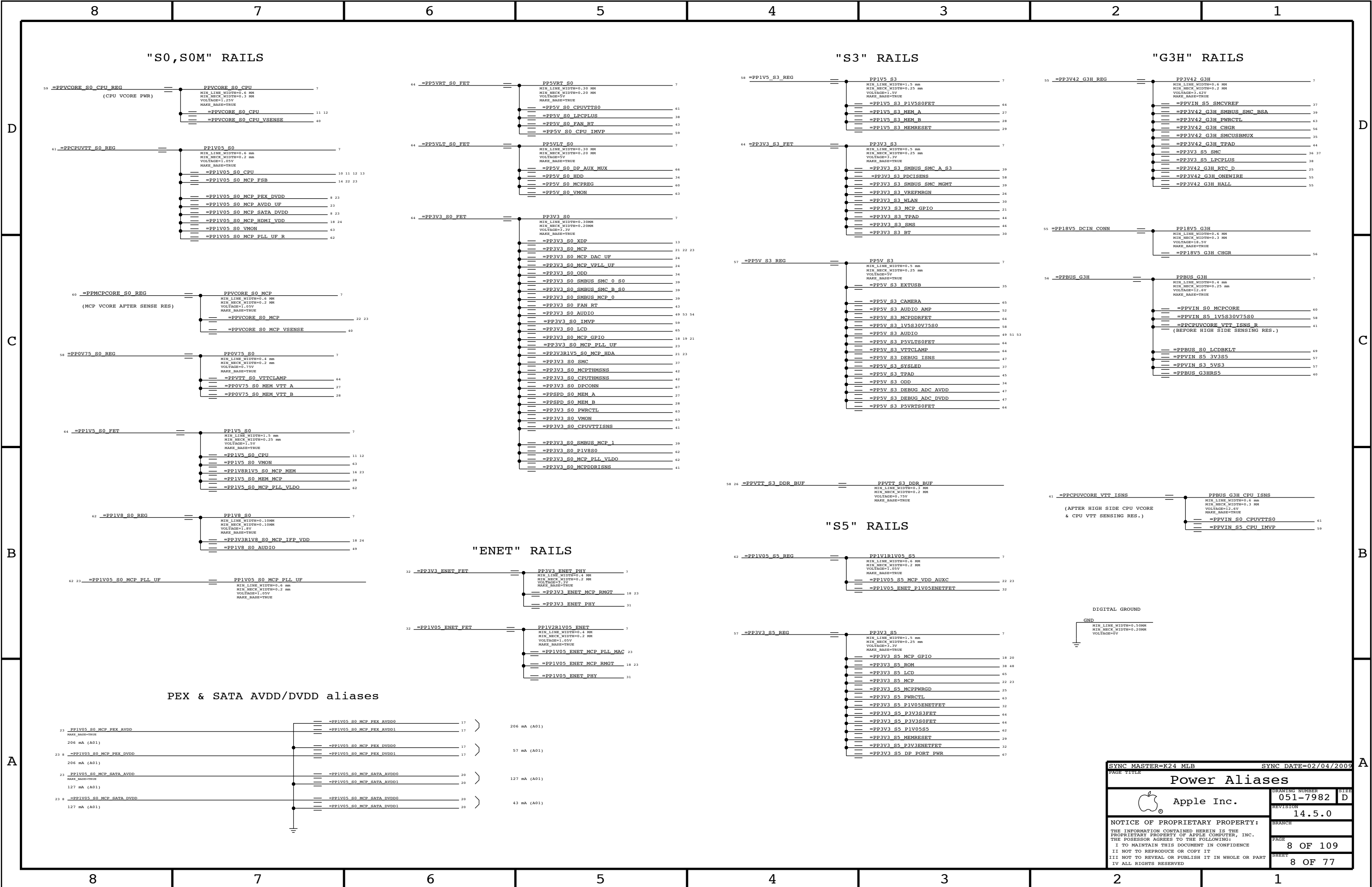
514-0690 IS PLASTIC VERSION OF 514-0691 METAL PART FOR MINI DP CONNECTOR
514-0688 IS PLASTIC VERSION OF 514-0689 METAL PART FOR USB CONNECTORS

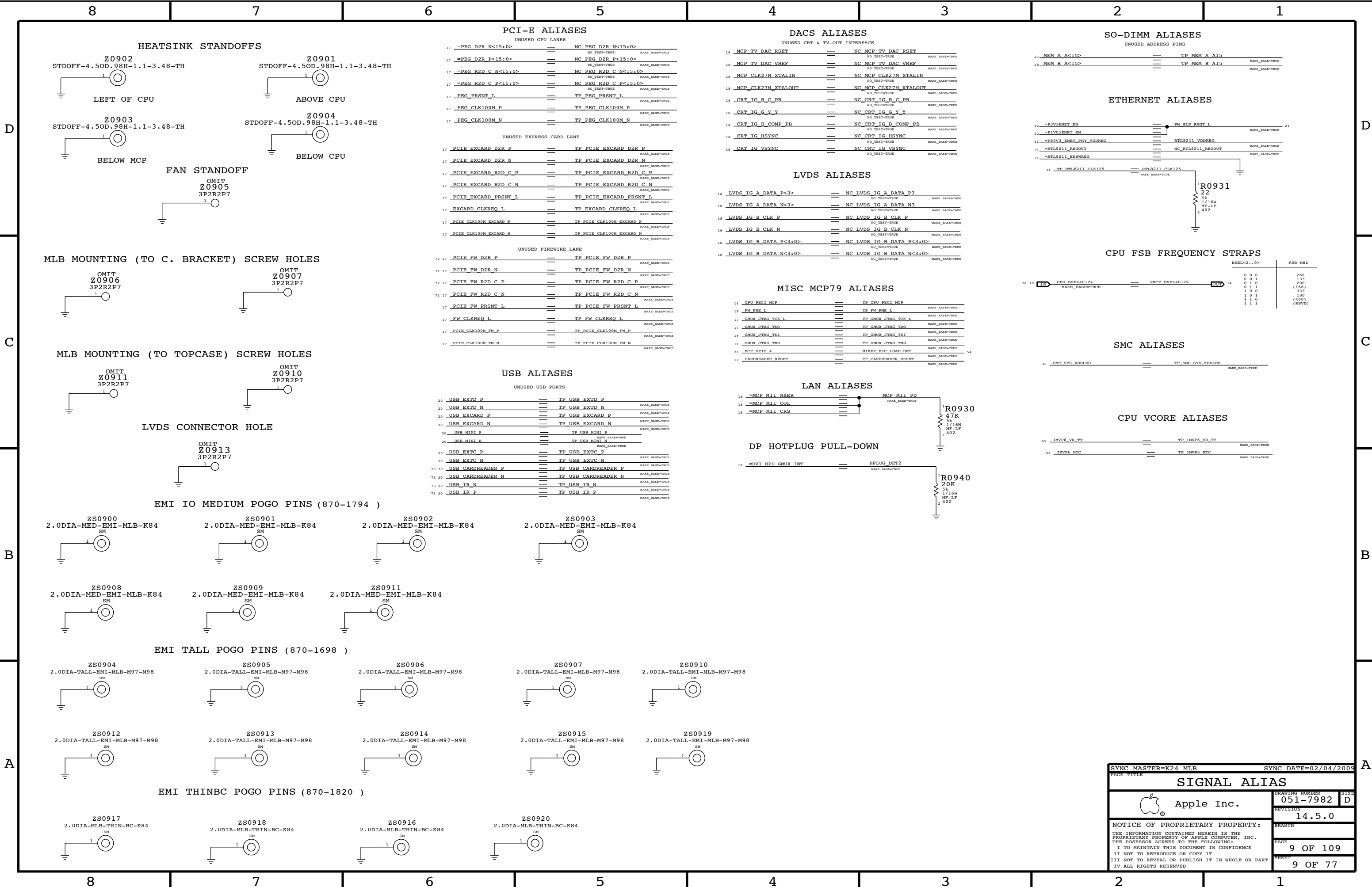
K84 BOARD STACK-UP

Top		SIGNAL
2		GROUND
3		SIGNAL(High Speed)
4		SIGNAL(High Speed)
5		GROUND
6		POWER
7		POWER
8		GROUND
9		SIGNAL(High Speed)
10		SIGNAL(High Speed)
11		GROUND
BOTTOM		SIGNAL

SYNC MASTER-K24 MLB		SYNC DATE=01/19/2009	
PAGE TITLE			
BOM Configuration			
 Apple Inc.		DRAWING NUMBER	
		051-7982	
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Functional Test Points											
D	FAN CONNECTORS FUNC_TEST		X16 WIRELESS CONN FUNC_TEST		POWER NETS FUNC_TEST						
	PP5VRT S0		PP3V3 S3_BT_F		PPVCORE S0_CPU						
	FAN_RT_PWM		CONN_PCIE_MINI_D2R_P		PPVCORE S0_MCP						
	FAN_RT_TACH		CONN_PCIE_MINI_D2R_N		PP0V75 S0						
	(NEED TO ADD 1 GND TP)		CONN_PCIE_MINI_R2D_P		PP1V05 S0						
	MIC_FUNC_TEST		CONN_PCIE_MINI_R2D_N		PP1V5 S0						
	BI_MIC_LO		PCIE_CLK100M_MINI_CONN_P		PP1V8 S0						
	BI_MIC_HI		PCIE_CLK100M_MINI_CONN_N		PP5VLT S0						
	BI_MIC_SHIELD		PP3V3_WLAN		PP5VRT S0						
	SPEAKER_FUNC_TEST		PCIE_WAKE_L		PP3V3 S0						
C	SPKRAMP_L_N_OUT		CONN_USB2_BT_P		PP1V5 S3						
	SPKRAMP_L_P_OUT		CONN_USB2_BT_N		PP3V3 S3						
	SPKRAMP_R_N_OUT		MINI_CLKREQ_Q_L		PP5V S3						
	SPKRAMP_R_P_OUT		MINI_RESET_CONN_L		PP1V1R1V05_S5						
	SPKRAMP_SUB_N_OUT		(NEED TO ADD 2 GND TP)		PP3V3 S5						
	SPKRAMP_SUB_P_OUT		IPD_FLEX_CONN_FUNC_TEST		PP3V42_G3H						
	PP3V3_LCDVDD_SW_F		PP3V3_S3_LDO		PPBUS_G3H						
	PP3V3_S0_LCD_F		PP18V5_S3		PP3V3_ENET_PHY						
	PPVOUT_S0_LCDBKLT		Z2_CS_L		PP1V2R1V05_ENET						
	LVDS_IG_DDC_CLK		Z2_DEBUG3		PP3V3_G3_RTC						
B	LVDS_IG_DDC_DATA		Z2_MOSI		PP3V3_WLAN						
	LVDS_IG_A_DATA_N<0>		Z2_MISO		PP5V_SW_ODD						
	LVDS_IG_A_DATA_P<0>		Z2_SCLK		PP5V_S0_HDD_FLT						
	LVDS_IG_A_DATA_N<1>		Z2_BOOST_EN		PP3V3_S5_AVREF_SMC						
	LVDS_IG_A_DATA_P<1>		Z2_HOST_INTN		PP18V5_S3						
	LVDS_IG_A_DATA_N<2>		Z2_CLKIN		PP3V3_S3_LDO						
	LVDS_IG_A_DATA_P<2>		Z2_KEY_ACT_L		PP3V3_LCDVDD_SW_F						
	LVDS_IG_A_CLK_F_N		Z2_RESET		PPVOUT_S0_LCDBKLT						
	LVDS_IG_A_CLK_F_P		PSOC_MISO		PP4V5_AUDIO_ANALOG						
	LED_RETURN_1		PSOC_MOSI		SMC_PM_G2_EN						
A	LED_RETURN_2		PSOC_SCLK		PM_SLP_S4_L						
	LED_RETURN_3		SMBUS_SMC_A_S3_SDA		PM_SLP_S3_L						
	LED_RETURN_4		SMBUS_SMC_A_S3_SCL		PP5V_S3_CAMERA_F						
	LED_RETURN_5		PSOC_F_CS_L		(NEED TO ADD 1 GND TP)						
	LED_RETURN_6		PICKB_L		DC_POWER_CONN_FUNC_TEST						
	PP5V_S3_CAMERA_F		KEYBOARD_CONN_FUNC_TEST		PP18V5_DCIN_FUSE (NEED 2 TP)						
	USB_CAMERA_CONN_P		PP3V3_S3		ADAPTER_SENSE						
	USB_CAMERA_CONN_N		PP3V42_G3H		(NEED TO ADD 2 GND TP)						
	(NEED TO ADD 5 GND TP)		WS_KBD1								
	SATA_ODD_CONN_FUNC_TEST		WS_KBD2								
A	PP5V_SW_ODD		WS_KBD3								
	SMC_ODD_DETECT		WS_KBD4								
	SATA_ODD_D2R_C_P		WS_KBD5								
	SATA_ODD_D2R_C_N		WS_KBD6								
	SATA_ODD_R2D_P		WS_KBD7								
	SATA_ODD_R2D_N		WS_KBD8								
	(NEED TO ADD 2 GND TP)		WS_KBD9								
	SATA_HDD/SIL_FUNC_TEST		WS_KBD10								
	PP5V_S0_HDD_FLT		WS_KBD11								
	SATA_HDD_R2D_P		WS_KBD12								
A	SATA_HDD_R2D_N		WS_KBD13								
	SATA_HDD_D2R_C_P		WS_KBD14								
	SATA_HDD_D2R_C_N		WS_KBD15_CAP								
	SYS_LED_ANODE_R		WS_KBD16_NUM								
	(NEED TO ADD 3 GND TP)		WS_KBD17								
	BATT_POWER_CONN_FUNC_TEST		WS_KBD18								
	SMBUS_SMC_BSA_SCL		WS_KBD19								
	SMBUS_SMC_BSA_SDA		WS_KBD20								
	SYS_DETECT_L		WS_KBD21								
	BATT_POS_F		WS_KBD22								
A	(NEED TO ADD 2 GND TP)		WS_KBD23								
	HALL_EFFECT_CONNECTOR_FUNC_TEST		WS_KBD_ONOFF_L								
	PP3V42_G3H		WS_LEFT_SHIFT_KBD								
	SMC_LID_R		WS_LEFT_OPTION_KBD								
			WS_CONTROL_KBD								
			(NEED TO ADD 1 GND TP)								
					PAGE TITLE						
					SYNC_MASTER=K24_MLB						
					SYNC_DATE=02/04/2009						
					FUNG TEST						
					DRAWING NUMBER 051-7982						
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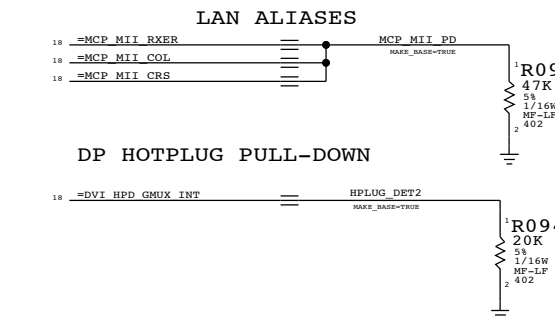




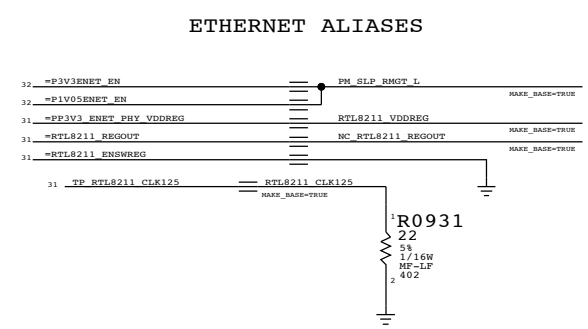
PCI-E ALIASES		
UNUSED GPU LANES		
17	=PEG D2R N<15:0>	== NC PEG D2R N<15:0>
17	=PEG D2R P<15:0>	== NC PEG D2R P<15:0>
17	=PEG R2D C N<15:0>	== NC PEG R2D C N<15:0>
17	=PEG R2D C P<15:0>	== NC PEG R2D C P<15:0>
17	PEG PRSNT L	== TP PEG PRSNT L
17	PEG CLK100M P	== TP PEG CLK100M P
17	PEG CLK100M N	== TP PEG CLK100M N
UNUSED EXPRESS CARD LANE		
17	PCIE EXCARD D2R P	== TP PCIE EXCARD D2R P
17	PCIE EXCARD D2R N	== TP PCIE EXCARD D2R N
17	PCIE EXCARD R2D C P	== TP PCIE EXCARD R2D C P
17	PCIE EXCARD R2D C N	== TP PCIE EXCARD R2D C N
17	PCIE EXCARD PRSNT L	== TP PCIE EXCARD PRSNT L
17	EXCARD CLKREQ L	== TP EXCARD CLKREQ L
17	PCIE CLK100M EXCARD P	== TP PCIE CLK100M EXCARD P
17	PCIE CLK100M EXCARD N	== TP PCIE CLK100M EXCARD N
UNUSED FIREWIRE LANE		
72 17	PCIE FW D2R P	== TP PCIE FW D2R P
72 17	PCIE FW D2R N	== TP PCIE FW D2R N
72 17	PCIE FW R2D C P	== TP PCIE FW R2D C P
72 17	PCIE FW R2D C N	== TP PCIE FW R2D C N
17	PCIE FW PRSNT L	== TP PCIE FW PRSNT L
17	FW CLKREQ L	== TP FW CLKREQ L
17	PCIE CLK100M FW P	== TP PCIE CLK100M FW P
17	PCIE CLK100M FW N	== TP PCIE CLK100M FW N
USB ALIASES		
UNUSED USB PORTS		
20	USB EXT D P	== TP USB EXT D P
20	USB EXT D N	== TP USB EXT D N
20	USB EXCARD P	== TP USB EXCARD P
20	USB EXCARD N	== TP USB EXCARD N
20	USB MINI P	== TP USB MINI P
20	USB MINI N	== TP USB MINI N
20	USB EXTC P	== TP USB EXTC P
20	USB EXTC N	== TP USB EXTC N
73 20	USB CARDREADER P	== TP USB CARDREADER P
73 20	USB CARDREADER N	== TP USB CARDREADER N
73 20	USB IR N	== TP USB IR N
73 20	USB IR P	== TP USB IR P

DACS ALIASES		
UNUSED CRT & TV-OUT INTERFACE		
18	MCP TV DAC RSET	== NC MCP TV DAC RSET
18	MCP TV DAC VREF	== NC MCP TV DAC VREF
18	MCP CLK27M XTALIN	== NC MCP CLK27M XTALIN
18	MCP CLK27M XTALOUT	== NC MCP CLK27M XTALOUT
18	CRT IG R C PR	== NC CRT IG R C PR
18	CRT IG G Y Y	== NC CRT IG G Y Y
18	CRT IG B COMP PB	== NC CRT IG B COMP PB
18	CRT IG HSYNC	== NC CRT IG HSYNC
18	CRT IG VSYNC	== NC CRT IG VSYNC
LVDS ALIASES		
18	LVDS IG A DATA P<3>	== NC LVDS IG A DATA P3
18	LVDS IG A DATA N<3>	== NC LVDS IG A DATA N3
18	LVDS IG B CLK P	== NC LVDS IG B CLK P
18	LVDS IG B CLK N	== NC LVDS IG B CLK N
18	LVDS IG B DATA P<3:0>	== NC LVDS IG B DATA P<3:0>
18	LVDS IG B DATA N<3:0>	== NC LVDS IG B DATA N<3:0>

MISC MCP79 ALIASES		
14	CPU PFCI MCP	== TP CPU PFCI MCP
19	FW PME L	== TP FW PME L
17	GMUX JTAG TCE L	== TP GMUX JTAG TCK L
17	GMUX JTAG TDO	== TP GMUX JTAG TDO
19	GMUX JTAG TDI	== TP GMUX JTAG TDI
19	GMUX JTAG TMS	== TP GMUX JTAG TMS
21	MCP GPIO 4	== HIKEY MIC LOAD DET
17	CARDREADER RESET	== TP CARDREADER RESET



SO-DIMM ALIASES		
UNUSED ADDRESS PINS		
27	MEM A A<15>	== TP MEM A A15
28	MEM B A<15>	== TP MEM B A15



CPU FSB FREQUENCY STRAPS		
BSEL<2..0>		FSB MHZ
0 0 0		266
0 0 1		333
0 1 0		260
0 1 1		(166)
1 0 0		333
1 0 1		400
1 1 0		(400)
1 1 1		(K8VD)

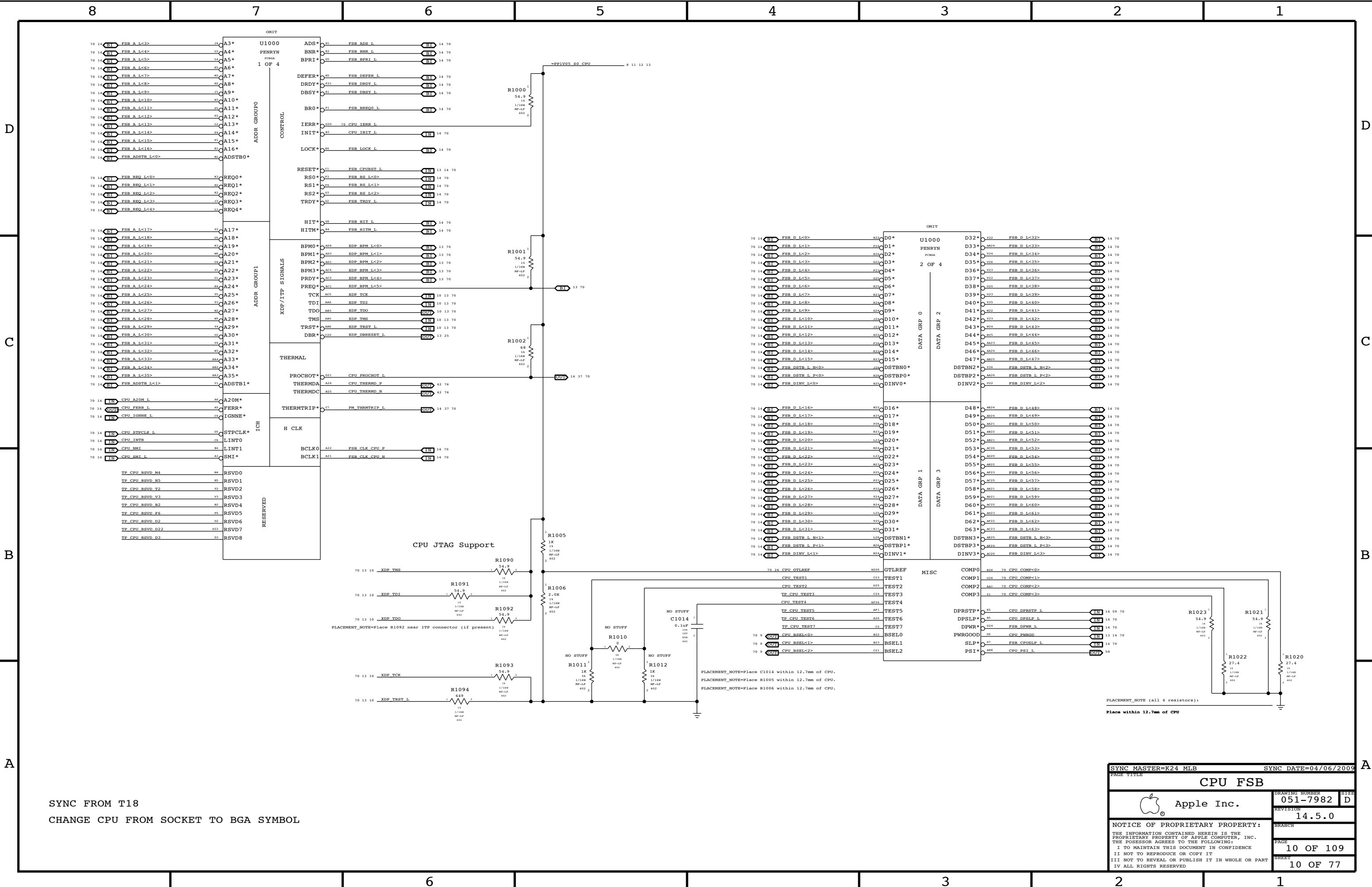
SMC ALIASES		
36	SMC SYS_KBDLED	== TP_SMC SYS_KBDLED

CPU VCORE ALIASES		
59	IMVP6_VR_TT	== TP_IMVP6_VR_TT
59	IMVP6_NTC	== TP_IMVP6_NTC

SYNC MASTER=K24 MLB

SYNC DATE=02/04/2009

SIGNAL ALIAS		
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	REVISION	14.5.0
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BRANCH	PAGE	9 OF 109
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SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC MASTER=K24 MLB		SYNC DATE=04/06/2009	
PAGE TITLE			
CPU FSB			
 Apple Inc.	DRAWING NUMBER	051-7982	SIZE D
	REVISION	14.5.0	
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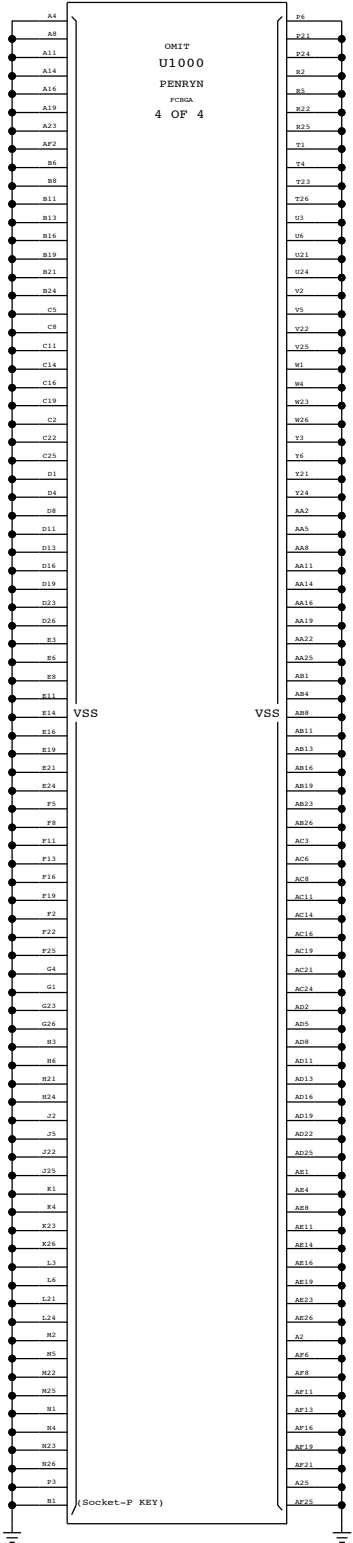
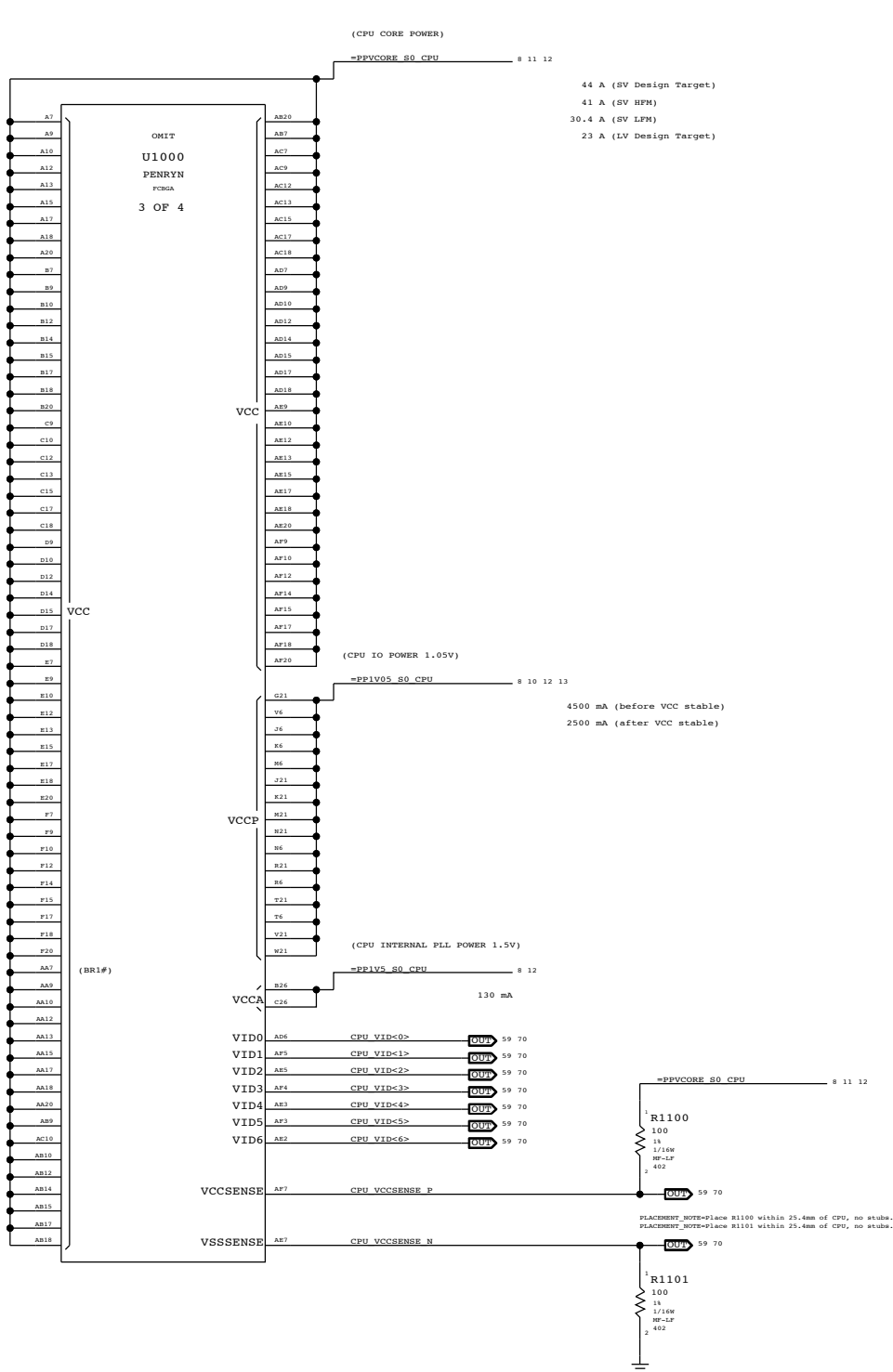
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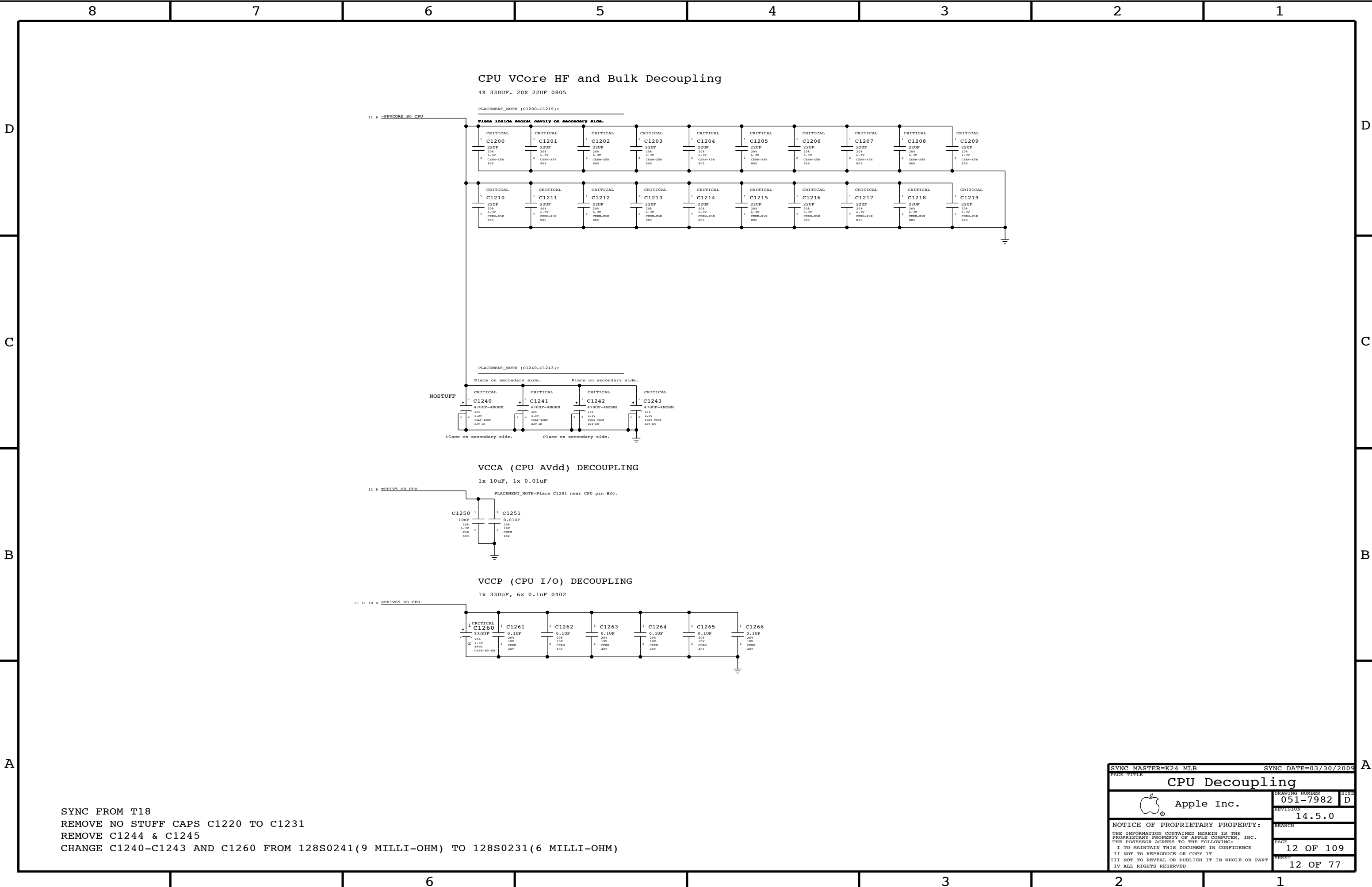
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SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.



SYNC MASTER=K24 MLB		SYNC DATE=04/06/2009	
PAGE TITLE			
CPU Power & Ground		DRAWING NUMBER	
 Apple Inc.		051-7982	SIZE
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		REVISION	
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SYNC FROM T18
REMOVE NO STUFF CAPS C1220 TO C1231
REMOVE C1244 & C1245
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

SYNC MASTER=K24 MLB		SYNC DATE=03/30/2009	
PAGE TITLE			
CPU Decoupling			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-7982		D
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	BRANCH		
	PAGE		12 OF 109
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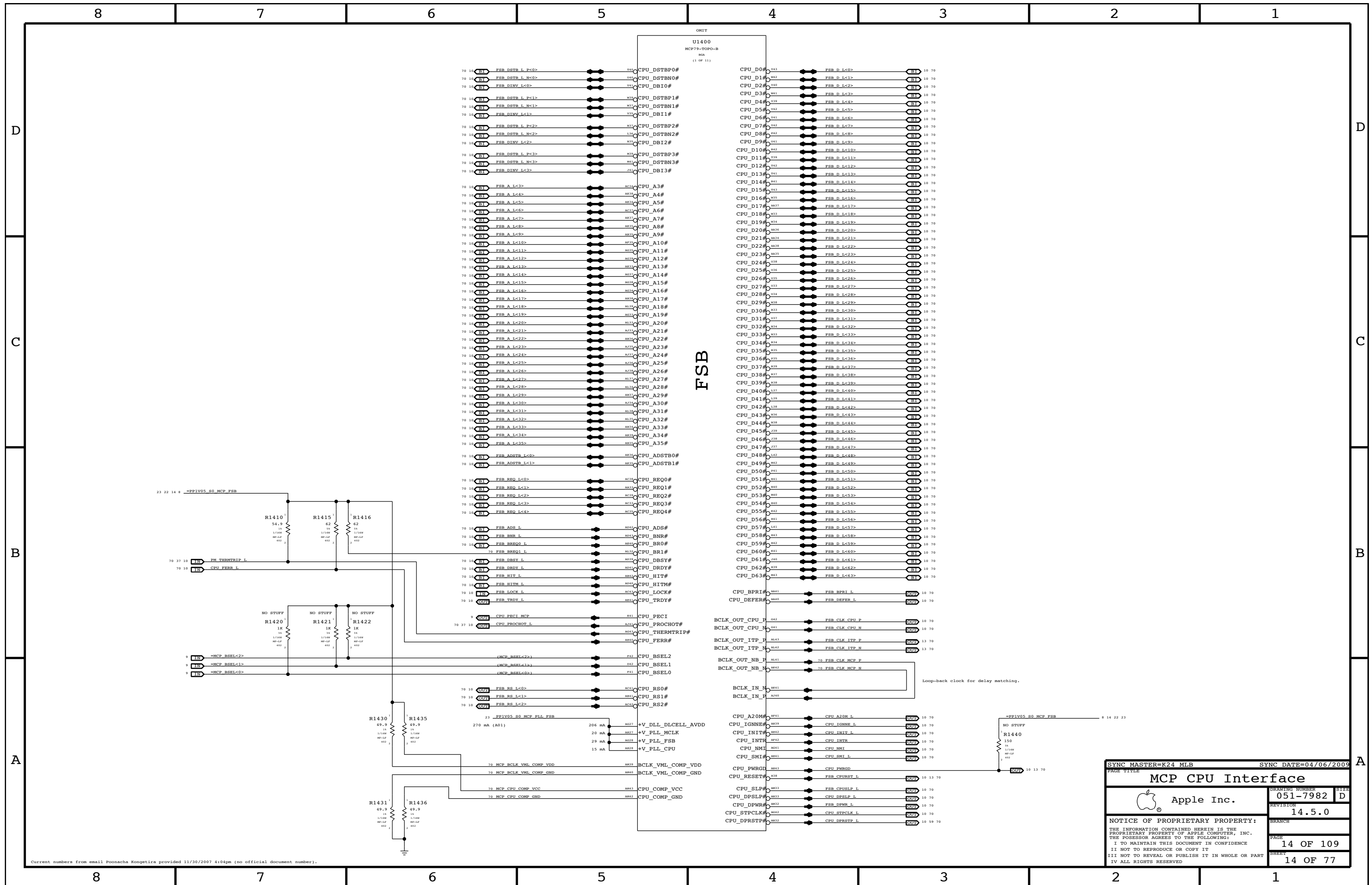
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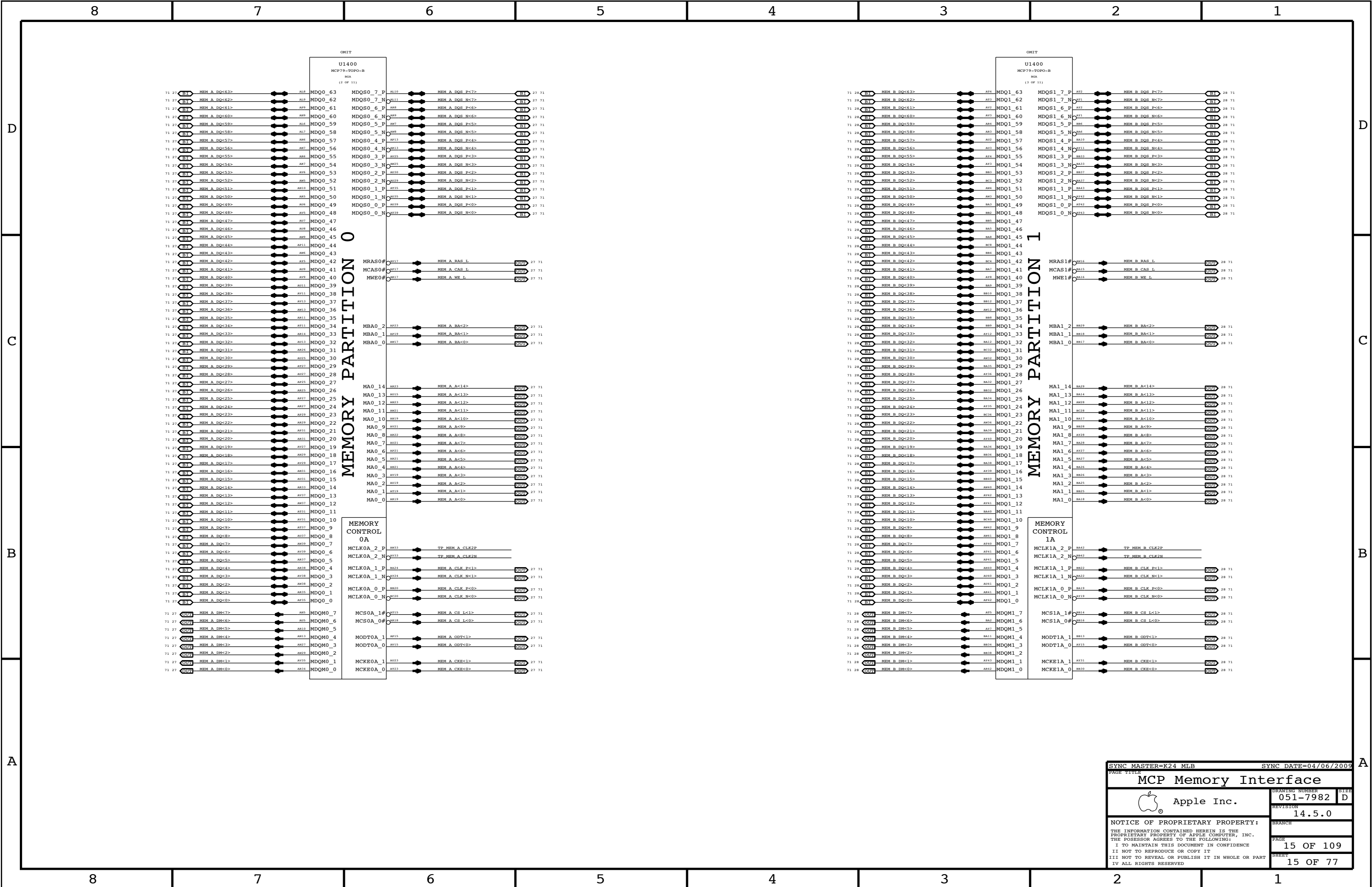
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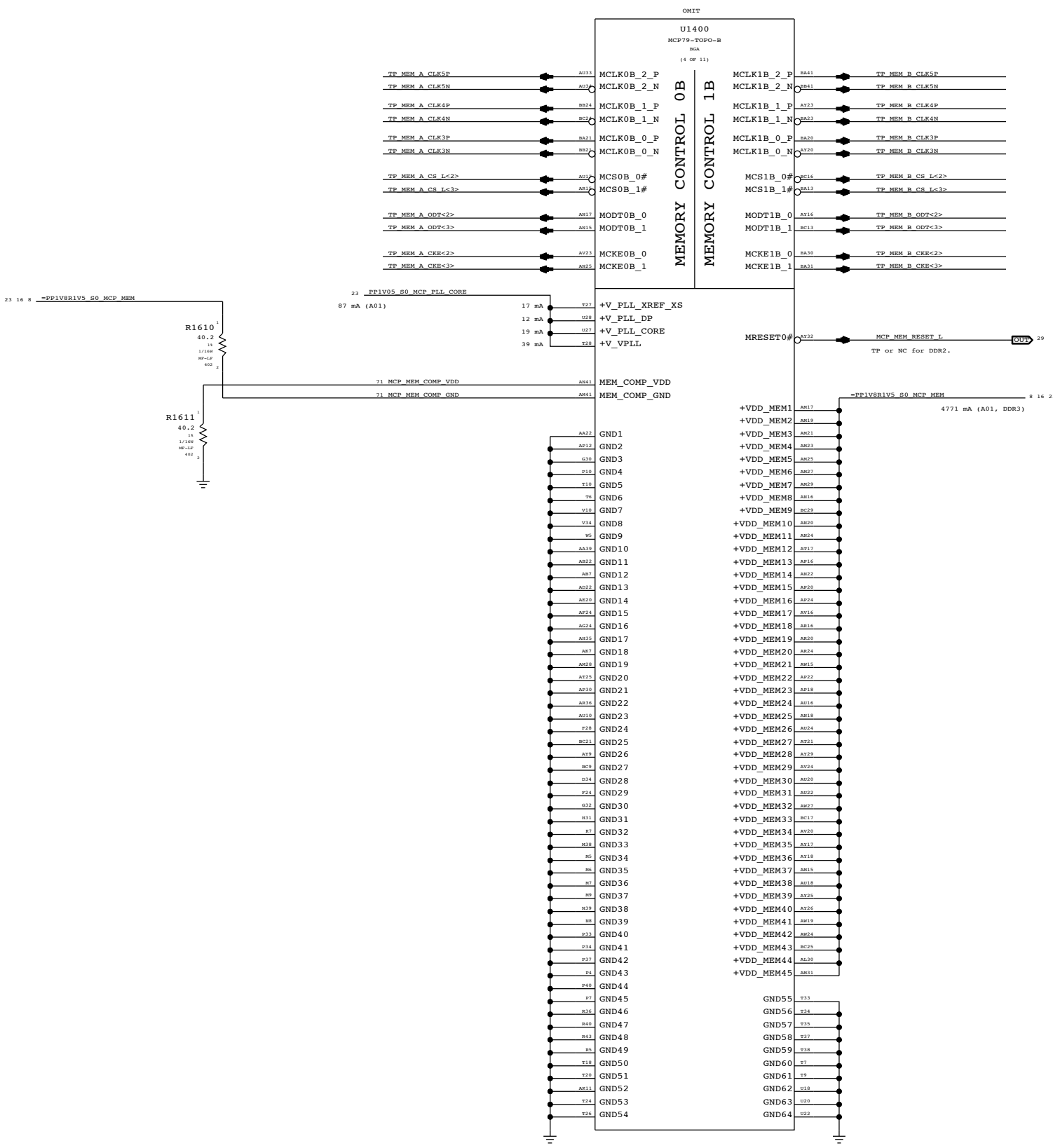
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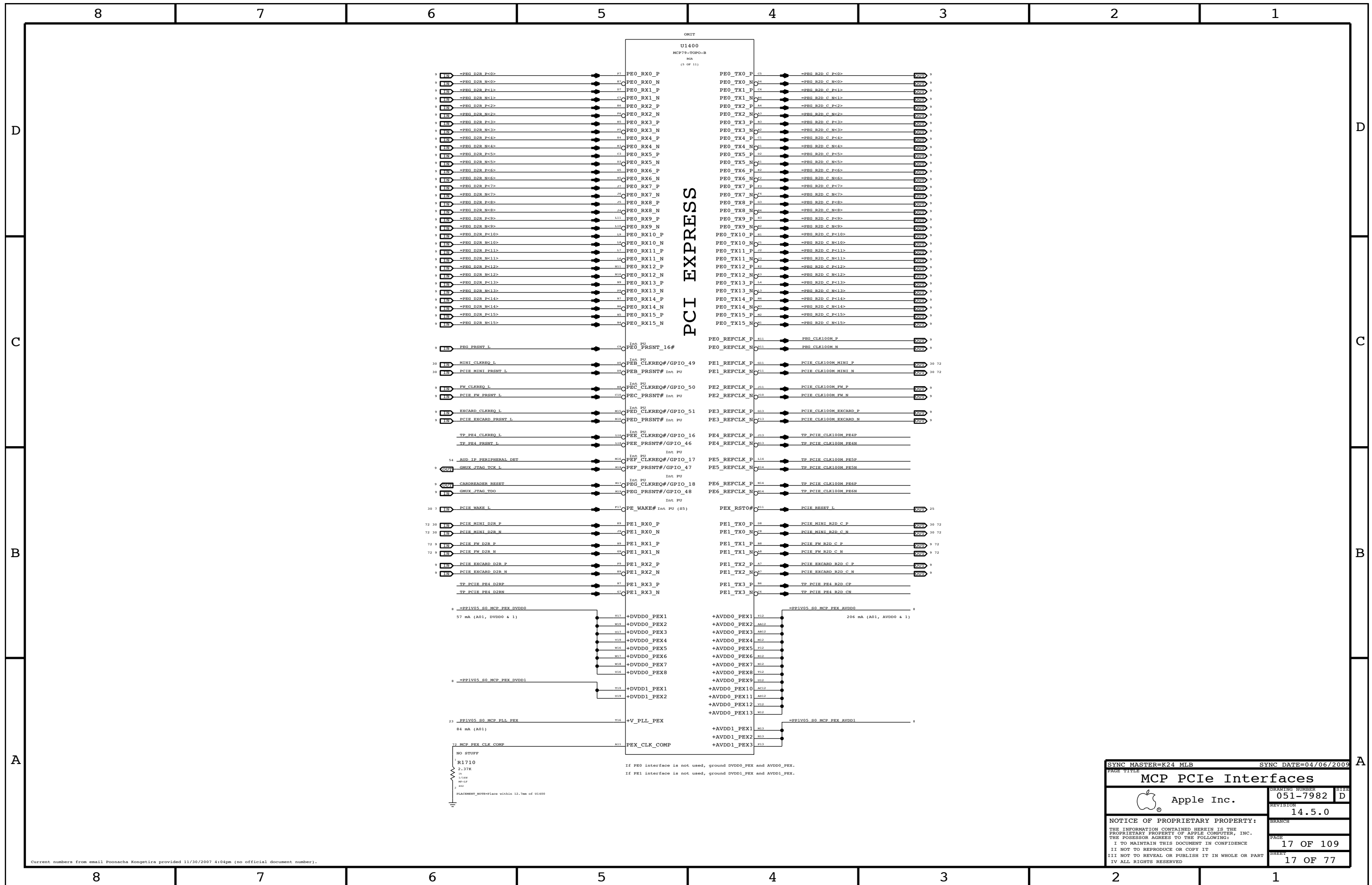
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SYNC MASTER=K24 MLB		SYNC DATE=04/06/2009	
PAGE TITLE			
MCP Memory Misc			
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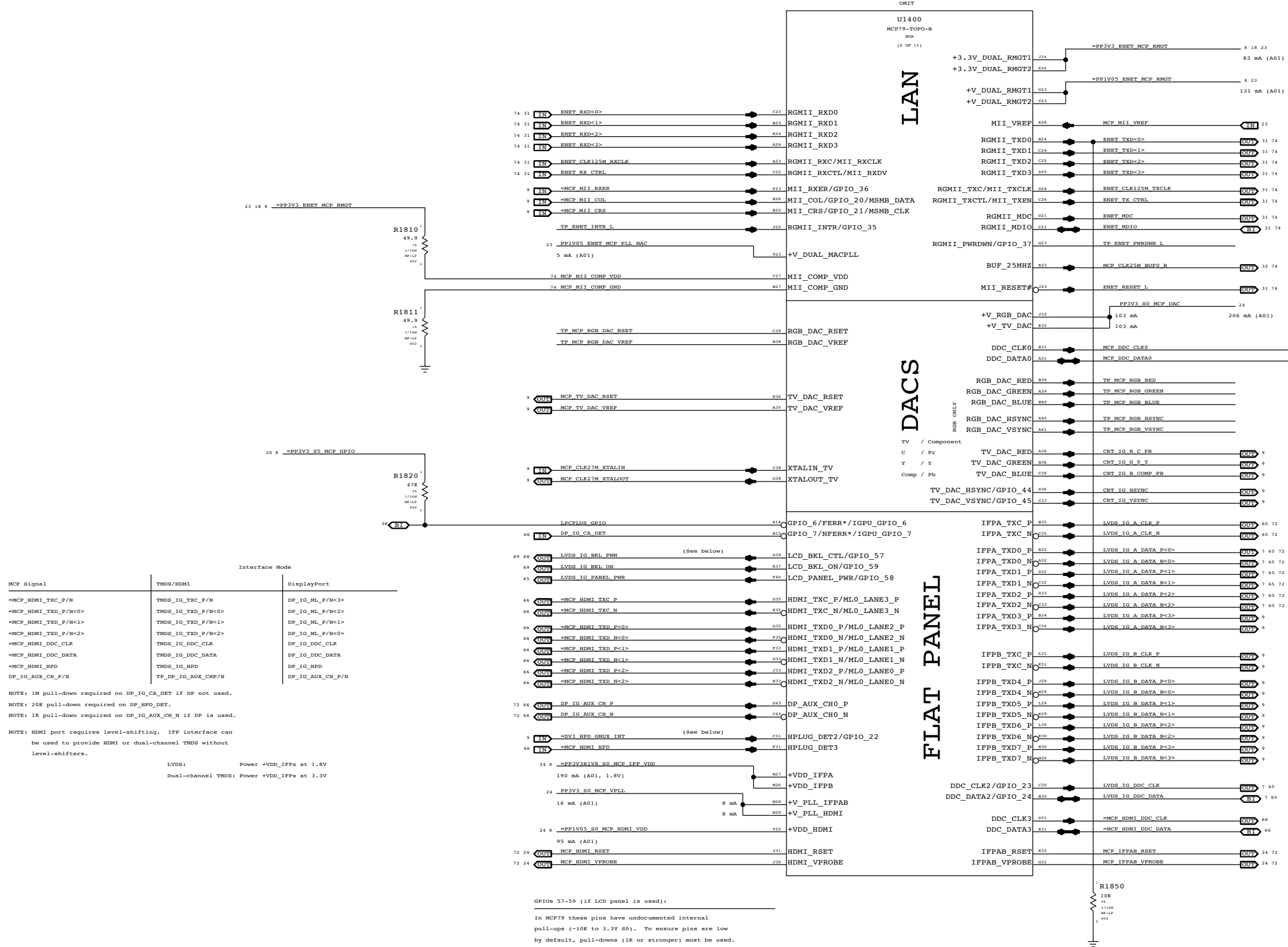
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MCP Signal	Interface Mode	
	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_SPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.
NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

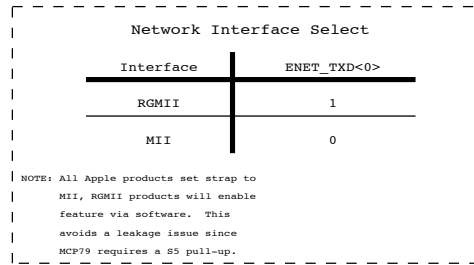
LVDS: Power +VDD_IFFx at 1.8V
Dual-channel TMDS: Power +VDD_IFFx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.



RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

SYNC MASTER=K24 MLB

SYNC DATE=04/06/2009

MCP Ethernet & Graphics

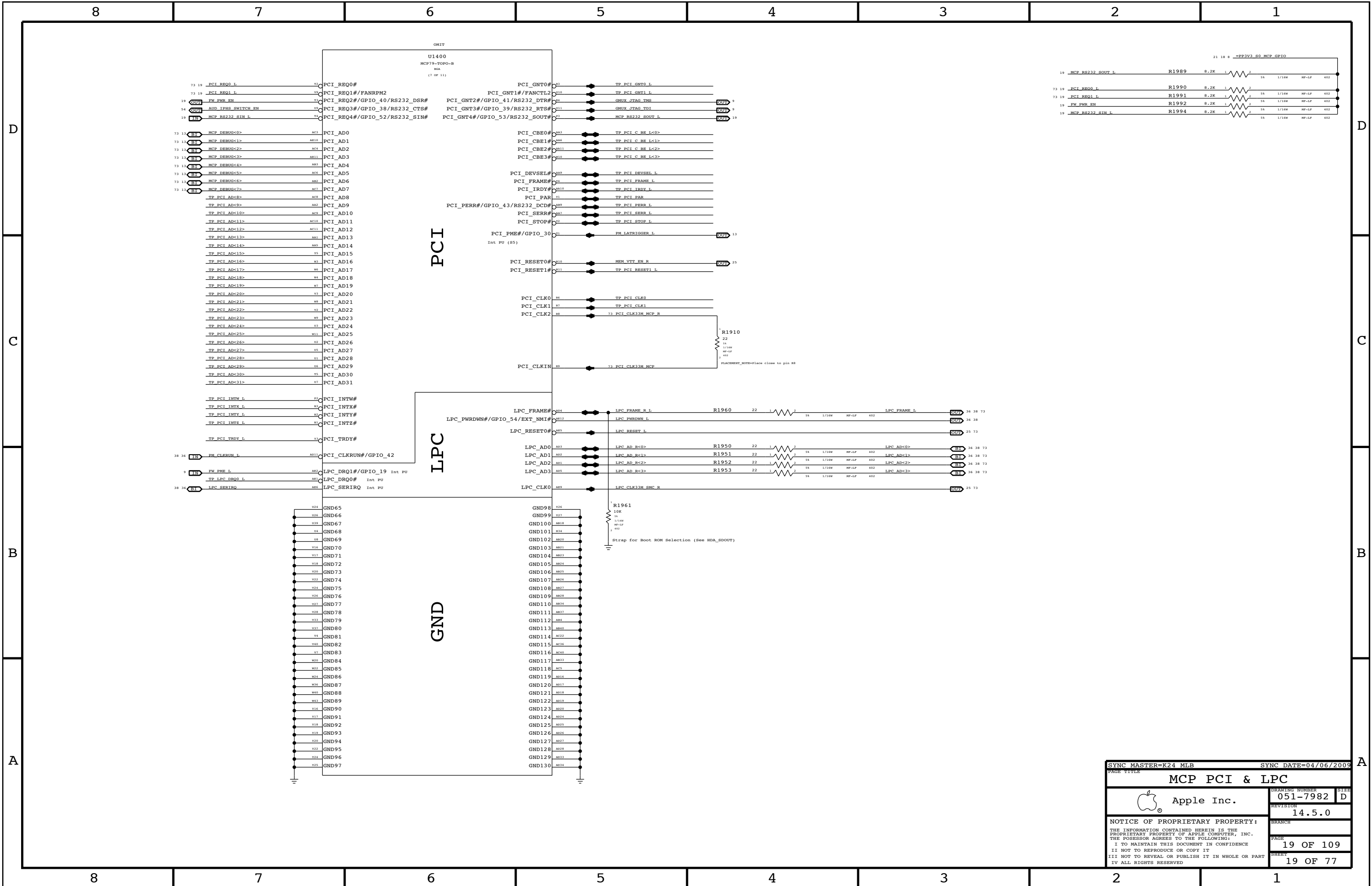
Apple Inc.

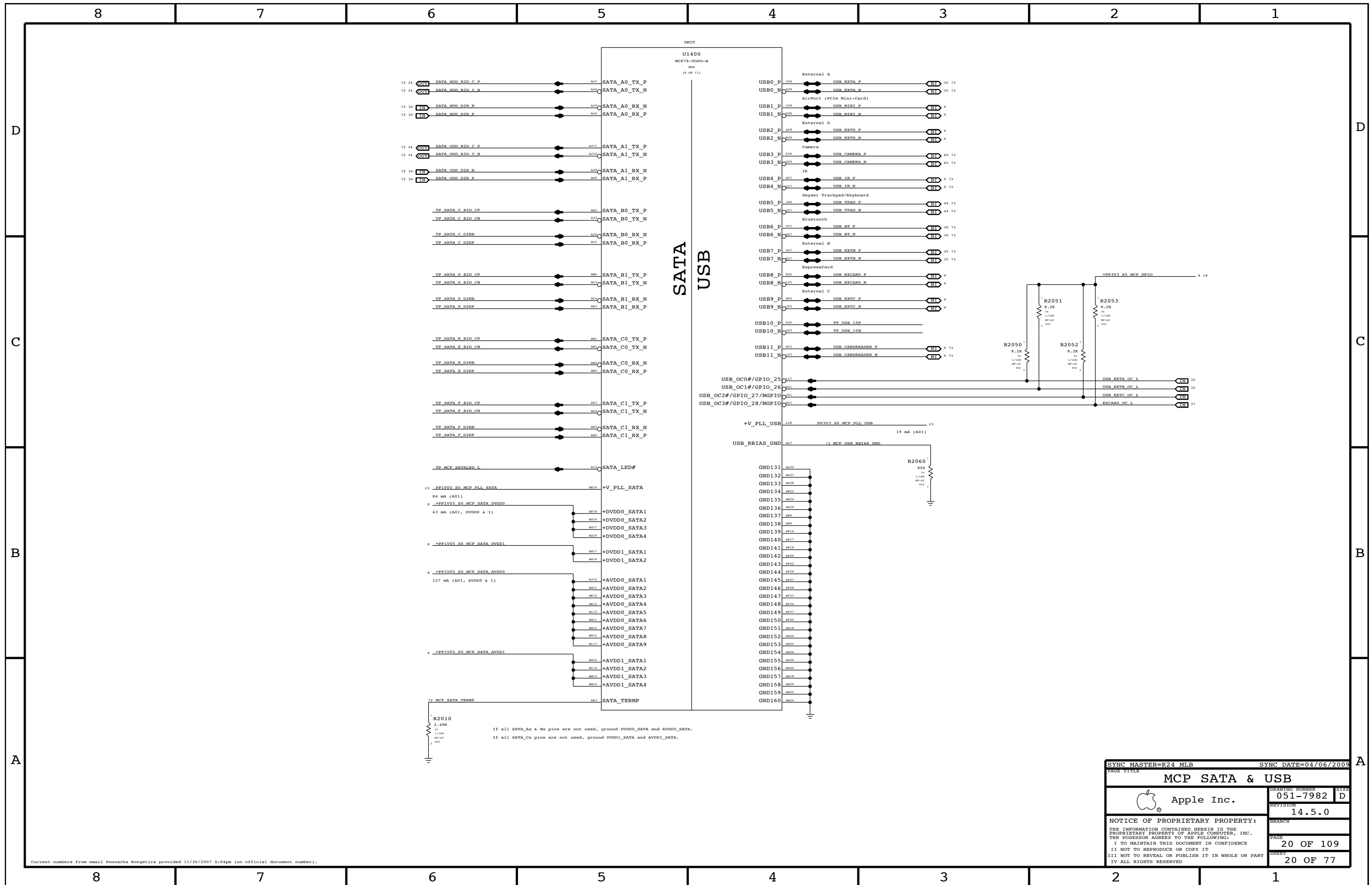
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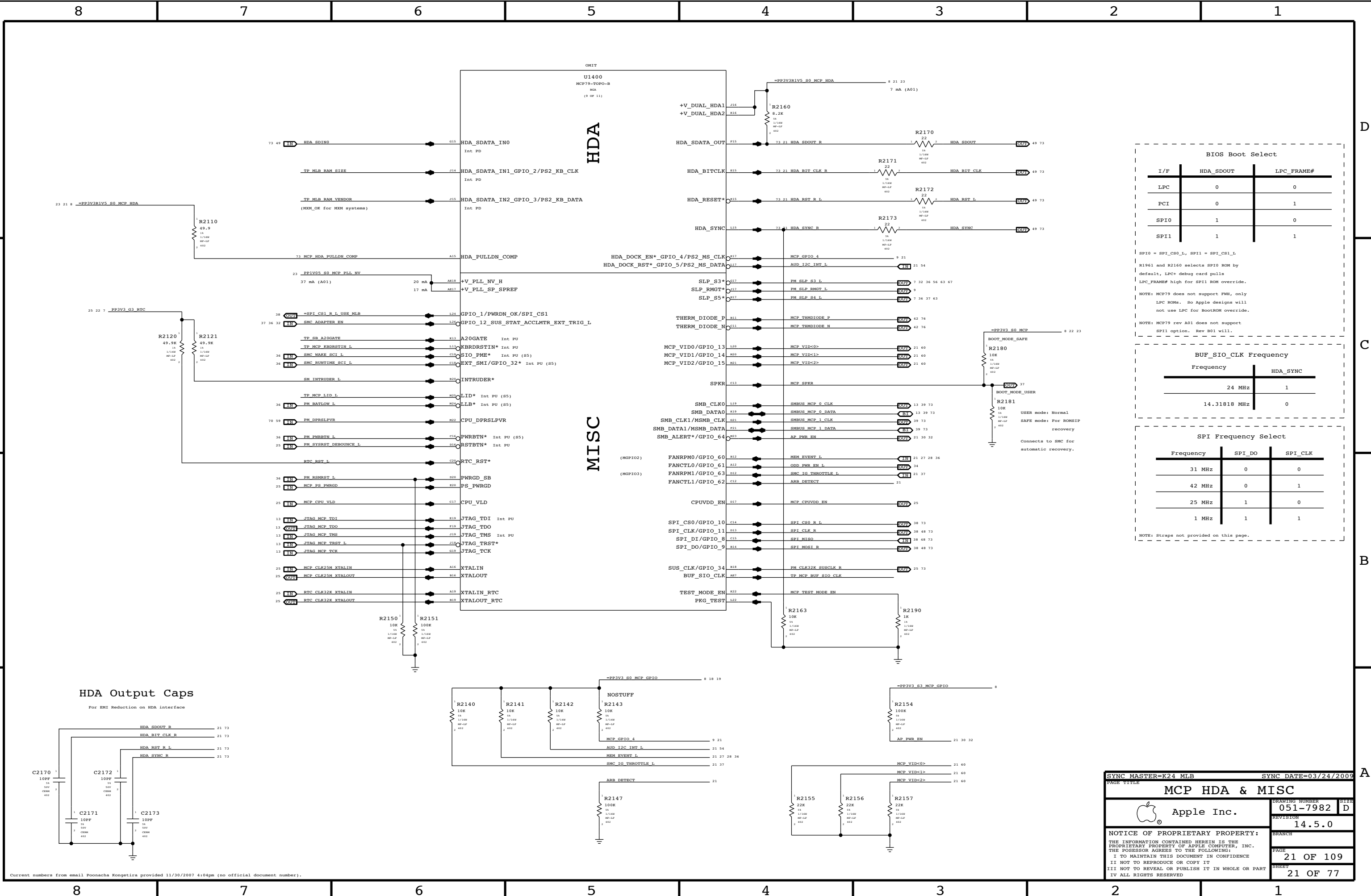
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BIOS Boot Select		
I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support PMH, only LPC ROMS. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

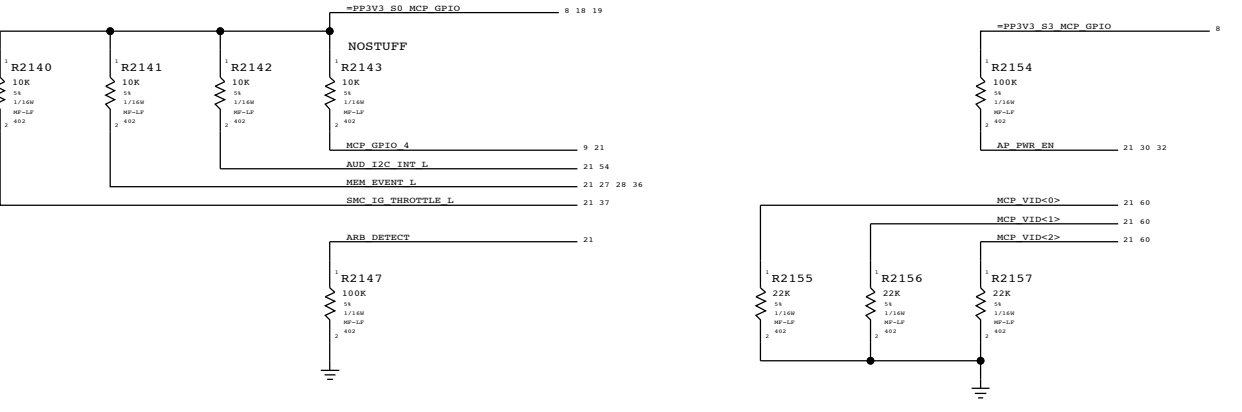
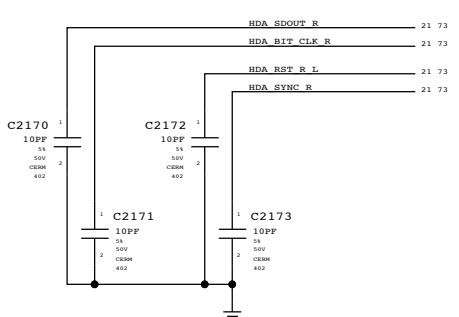
BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select		
Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

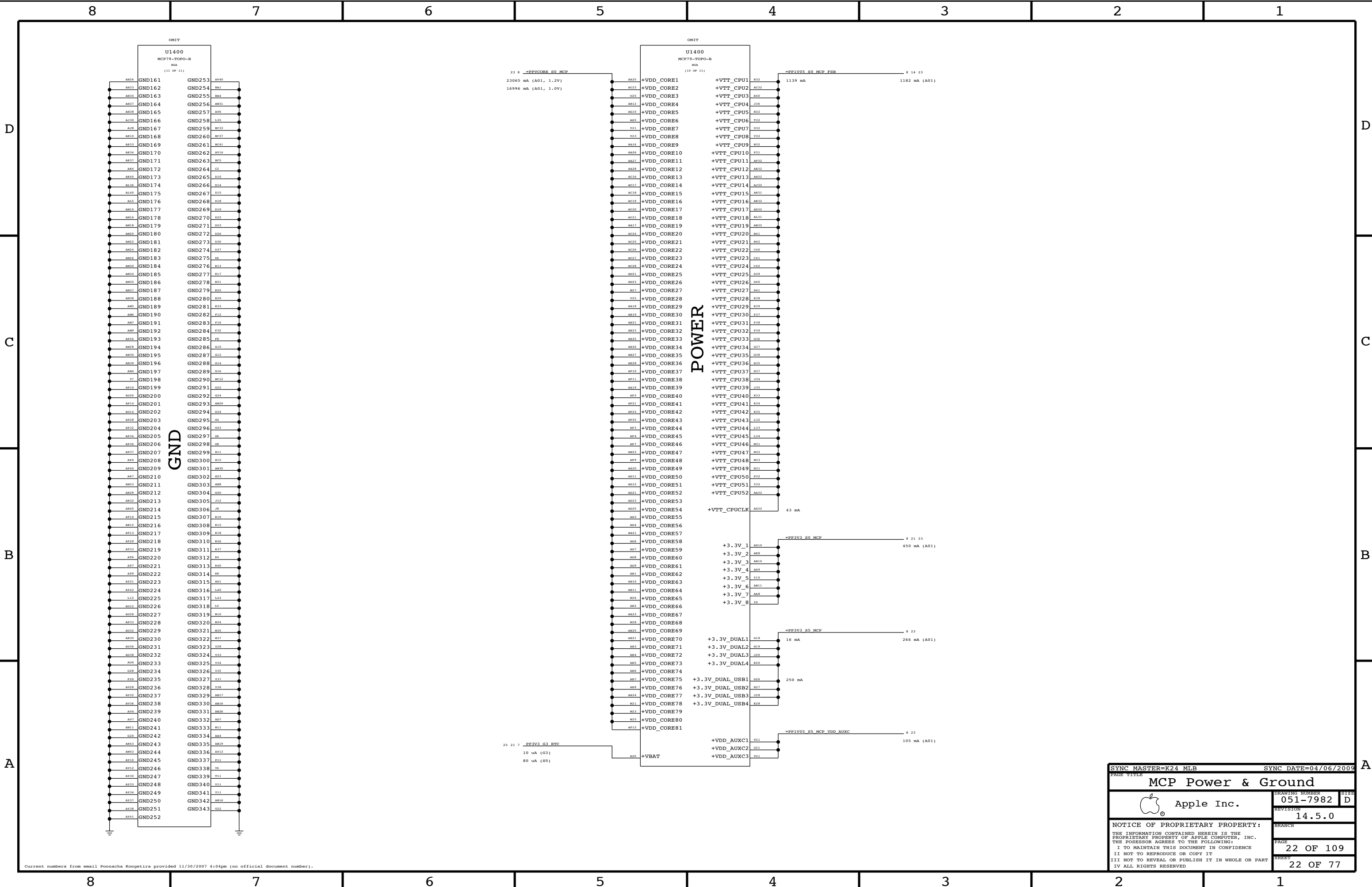
For EMI Reduction on HDA interface



SYNC MASTER=K24 MLB

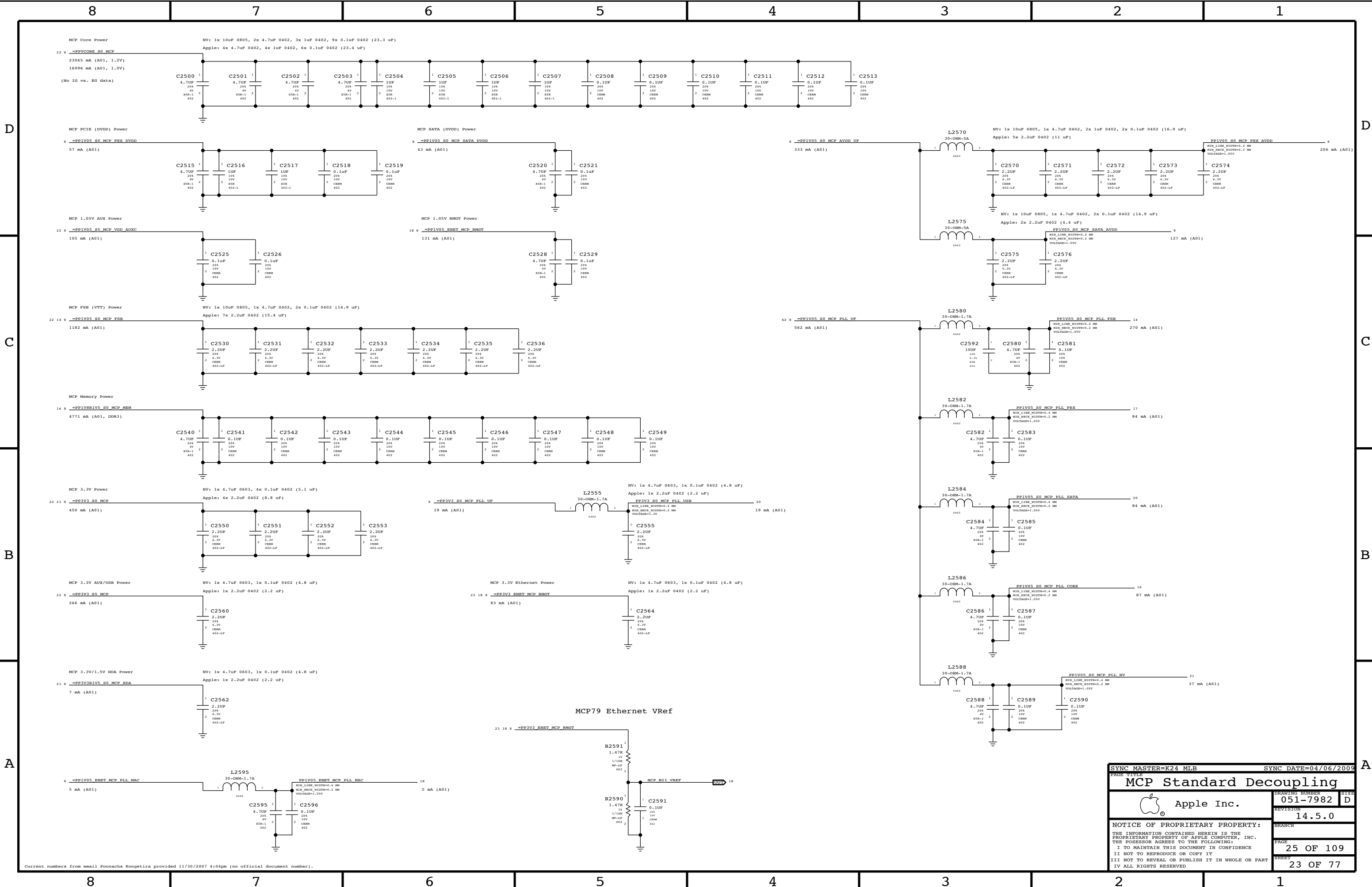
SYNC DATE=03/24/2009

MCP HDA & MISC		
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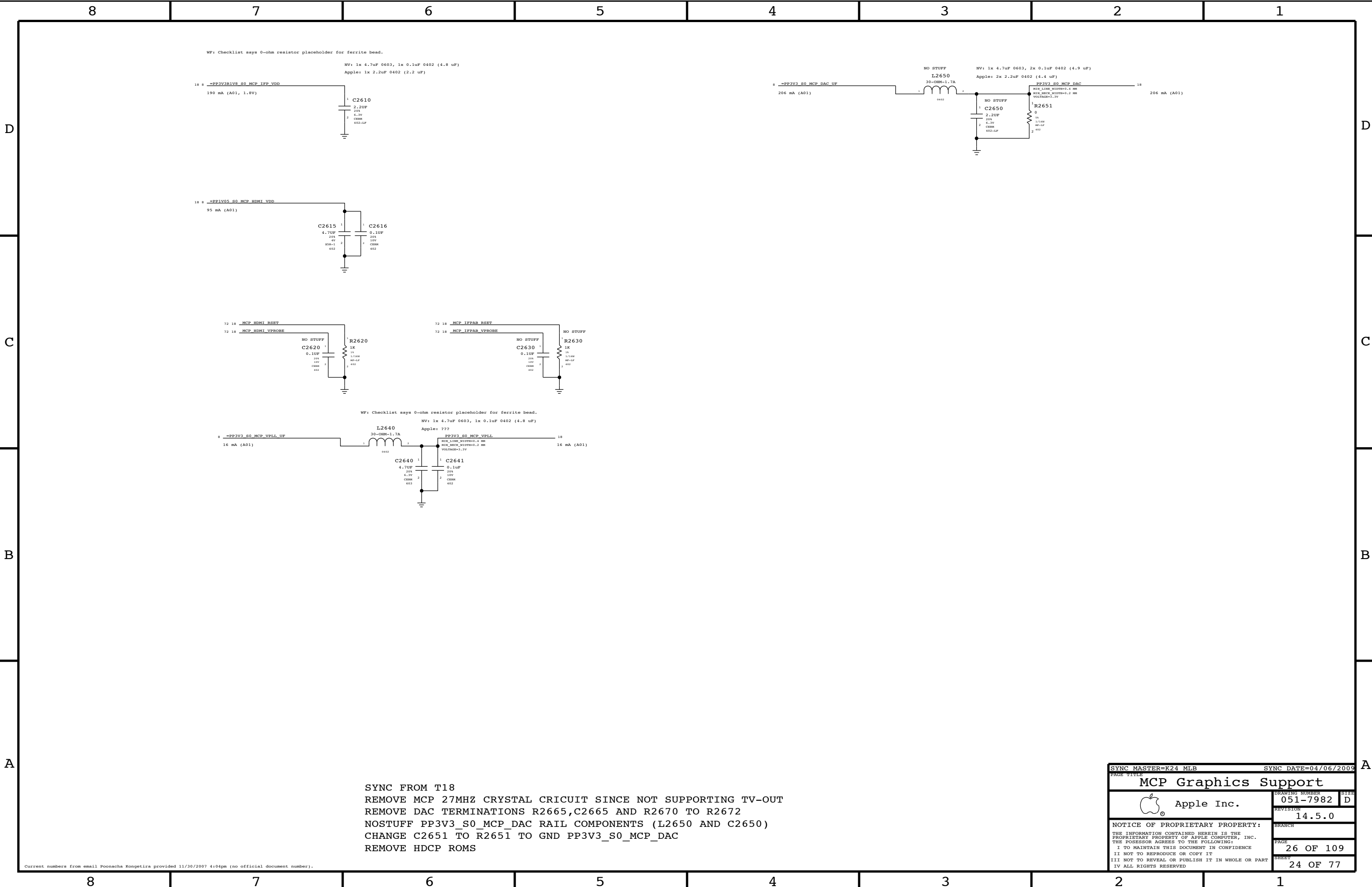
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC MASTER=K24 MLB		SYNC DATE=04/06/2009	
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MCP Power & Ground			
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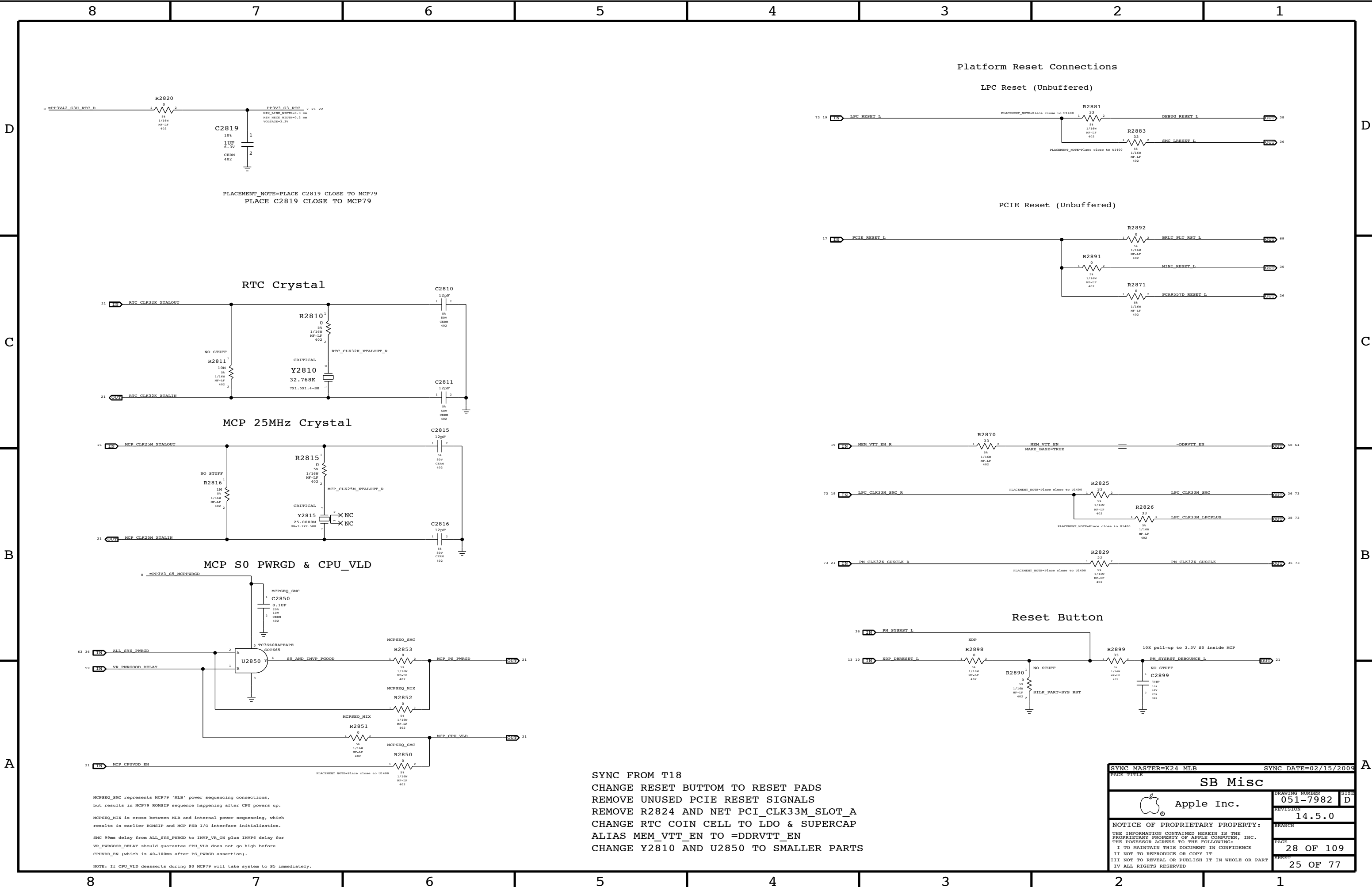
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MCP Standard Decoupling			
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SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC
REMOVE HDCP ROMS

SYNC MASTER=K24 MLB		SYNC DATE=04/06/2009	
PAGE TITLE			
MCP Graphics Support			
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SYNC FROM T18
CHANGE RESET BUTTON TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE Y2810 AND U2850 TO SMALLER PARTS

PAGE TITLE		DRAWING NUMBER		SIZE	
SB Misc		051-7982		D	
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Page Notes

Power aliases required by this page:

- ~PP3V3_S3_VREFMRGN
- ~PP3V3_S5_VREFMRGN
- ~PPVTT_S3_DDR_BUF

Signal aliases required by this page:

- ~I2C_VREFDACS_SCL
- ~I2C_VREFDACS_SDA
- ~I2C_PCA9557D_SCL
- ~I2C_PCA9557D_SDA

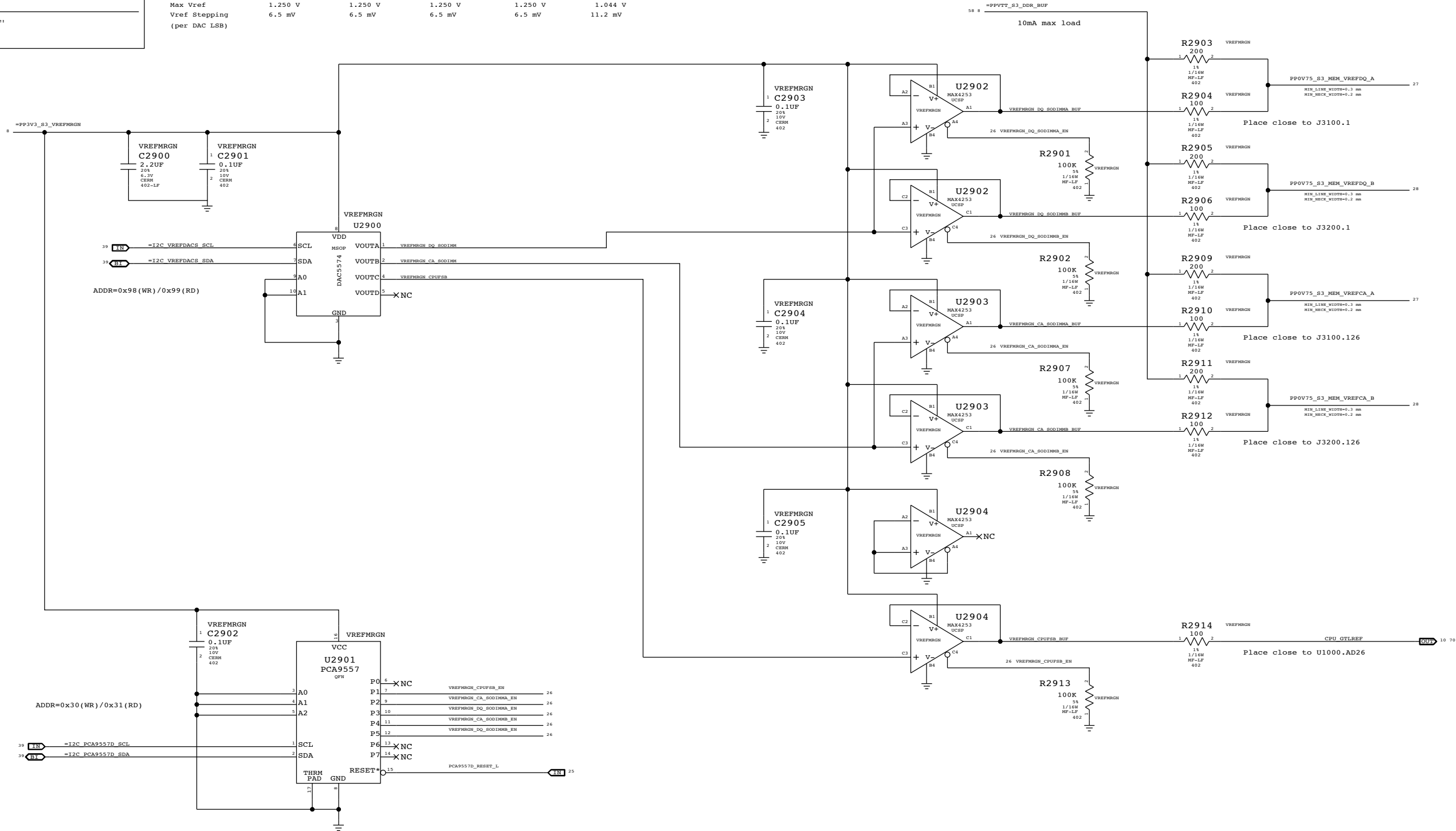
BOM options provided by this page:

VREFMRGN

NO_VREFMRGN

	MEM A VREF DQ		MEM A VREF CA		MEM B VREF DQ		MEM B VREF CA		CPU FSB VREF	
DAC channel	A	B	A	B	A	B	C			
Min DAC code	0x00	0x00	0x00	0x00	0x00	0x00	0x00			
Max DAC code	0x87	0x87	0x87	0x87	0x87	0x87	0x55			
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA			
Max source I	5 mA	5 mA	5 mA	5 mA	5 mA	5 mA	0.52 mA			
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V			
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V			
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V			
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV			

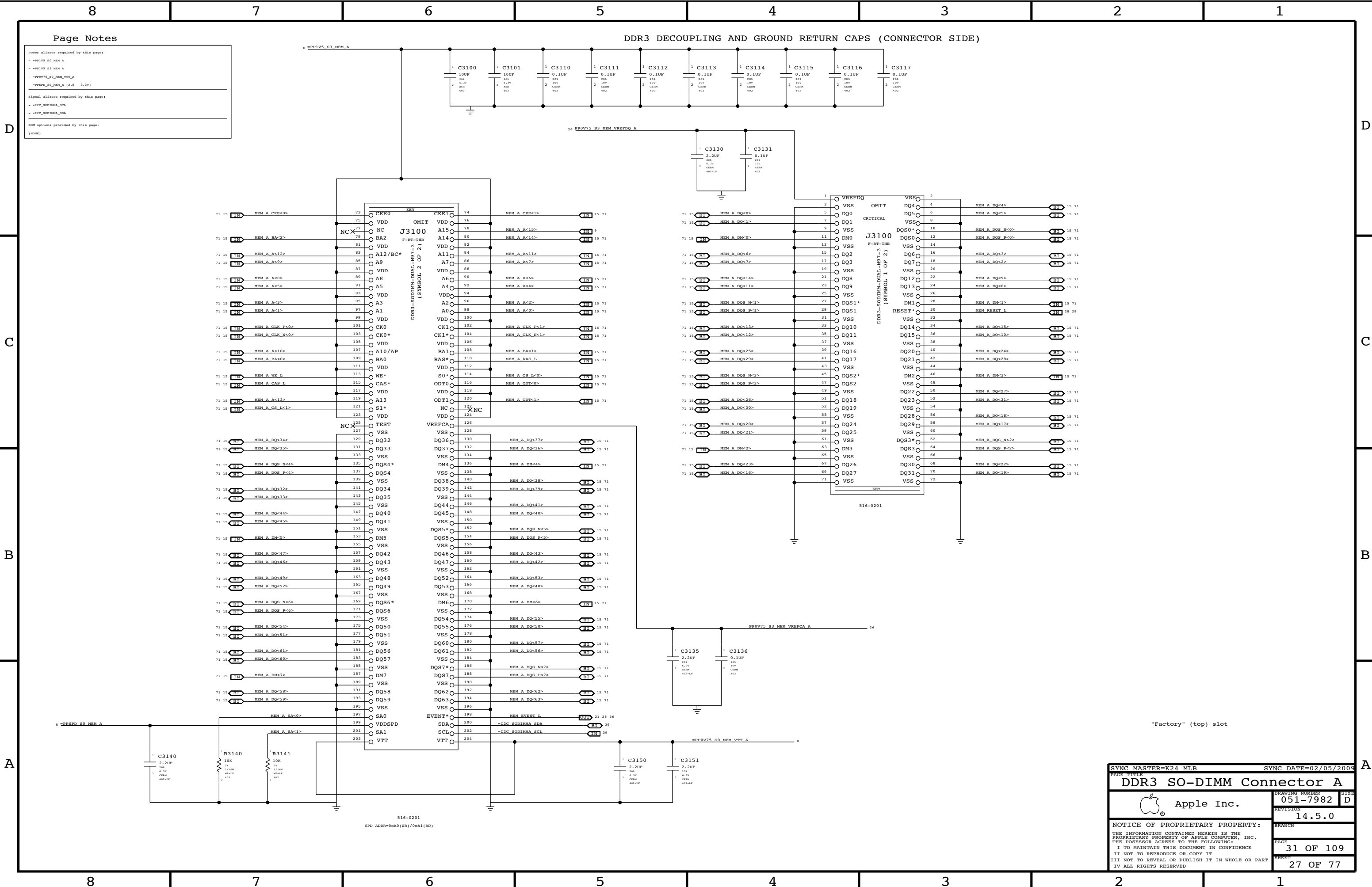
SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TP51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LP	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LP	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LP	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LP	R2911	CRITICAL	NO_VREFMRGN

SYNC MASTER=K24 MLB		SYNC DATE=04/06/2009	
PAGE TITLE			
FSB/DDR3 Vref Margining			
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Page Notes

Power aliases required by this page:

- PP1V5_S0_MEM_A
- PP1V5_S0_MEM_A
- PP0V75_S0_MEM_VTT_A
- PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- I2C_SODIMM_SCL
- I2C_SODIMM_SDA

DEM options provided by this page:

(NONE)

SYNC MASTER=K24 MLB

SYNC DATE=02/05/2009

DDR3 SO-DIMM Connector A

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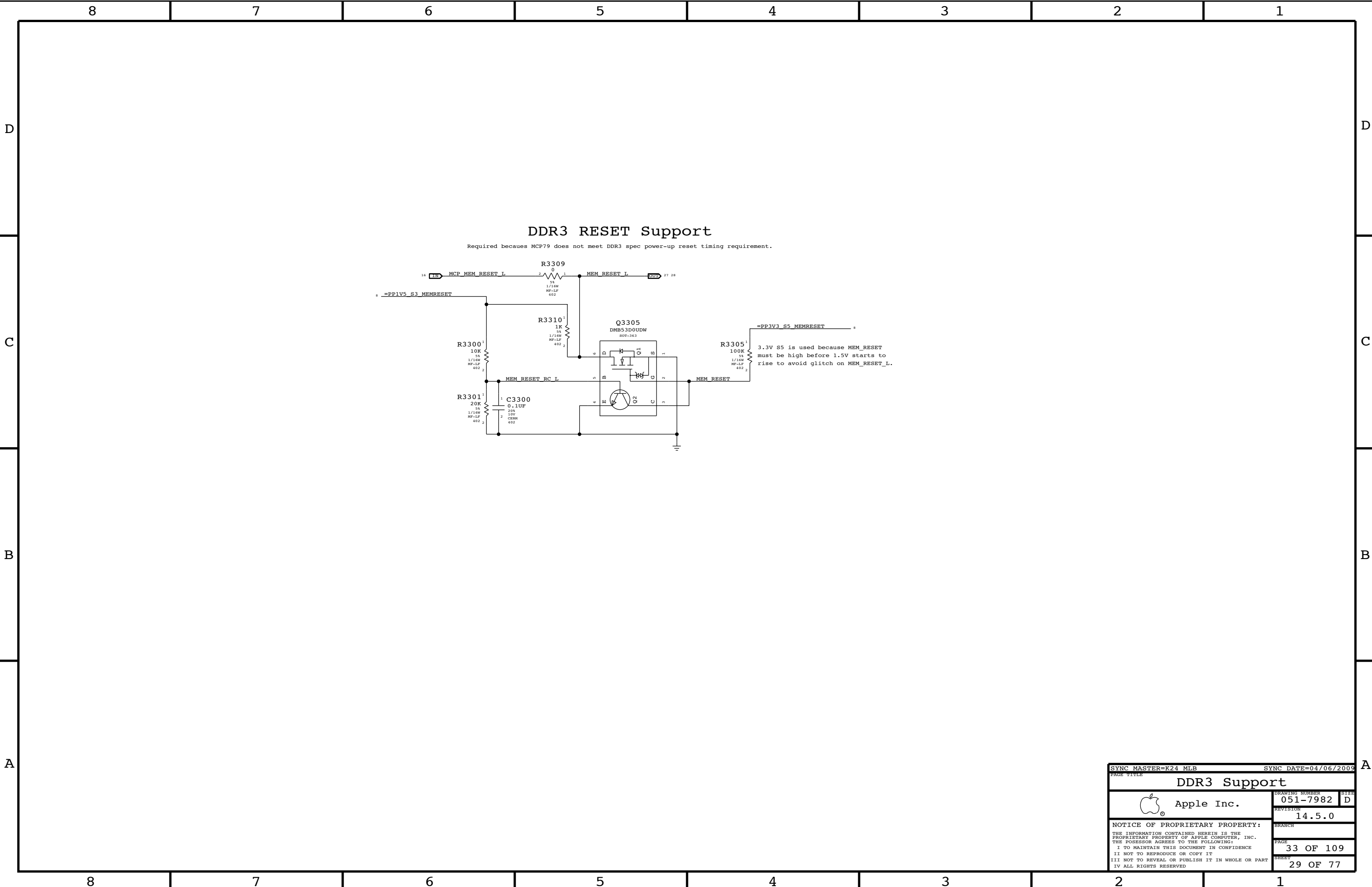
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"Factory" (top) slot



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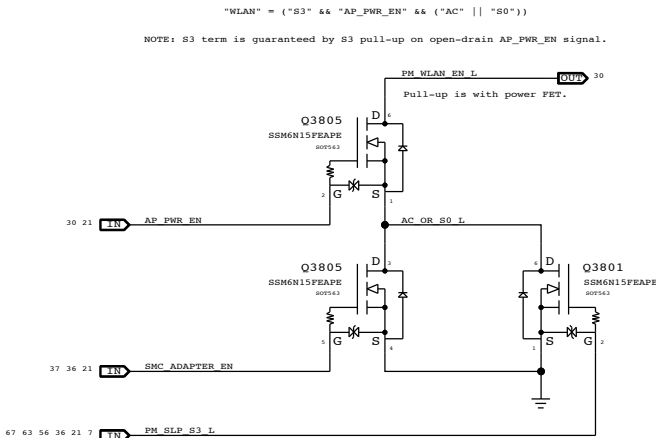
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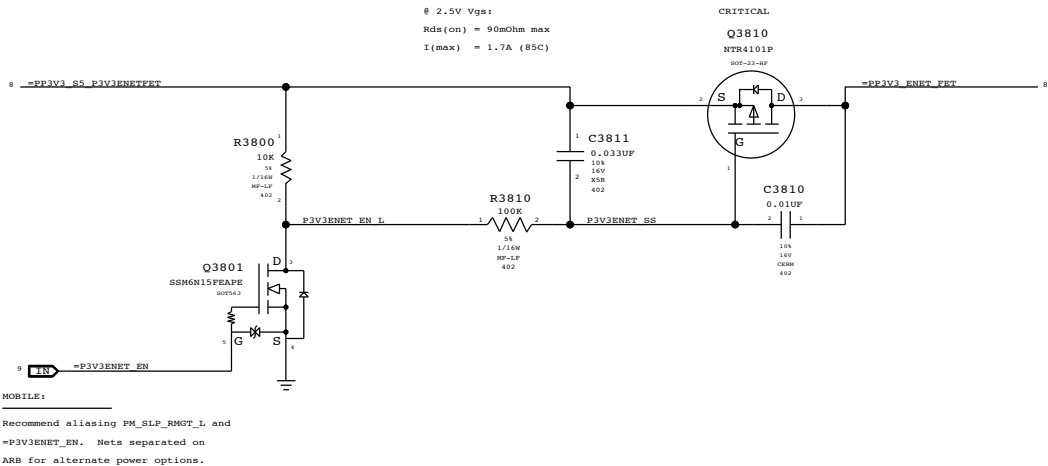
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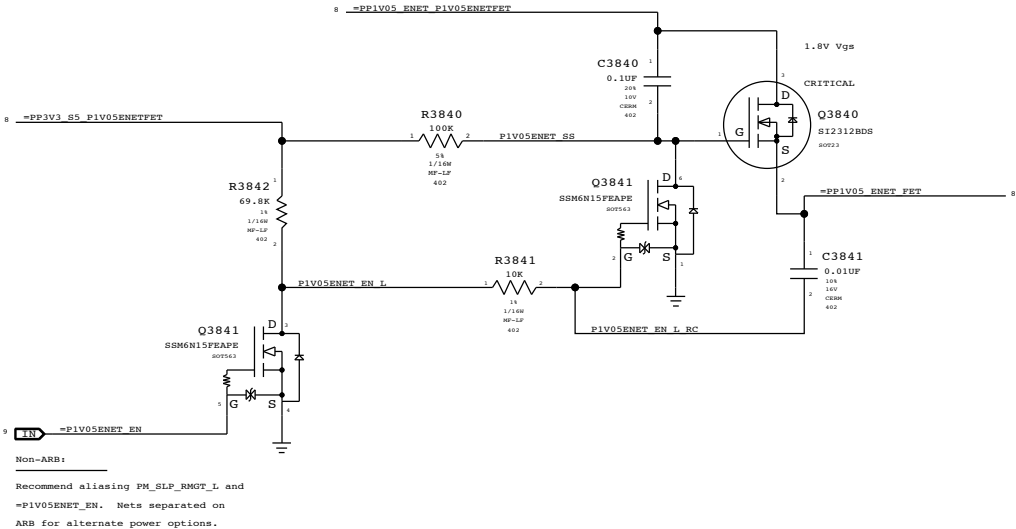
WLAN Enable Generation



3.3V ENET FET

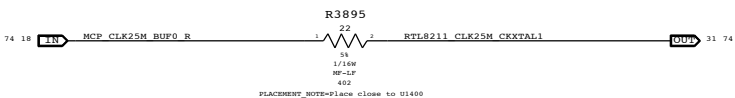


1.05V ENET FET

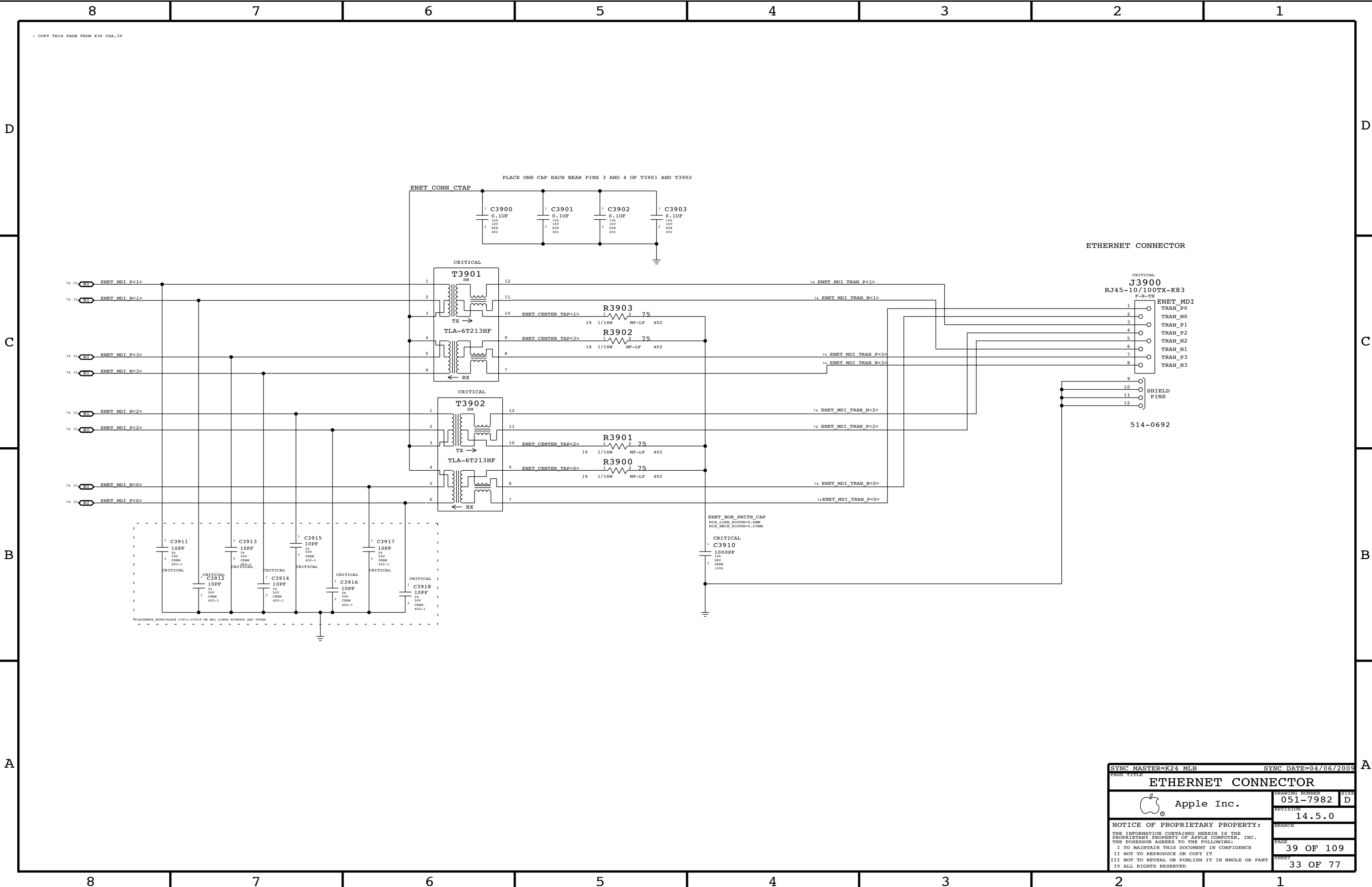


RTL8211 25MHz Clock

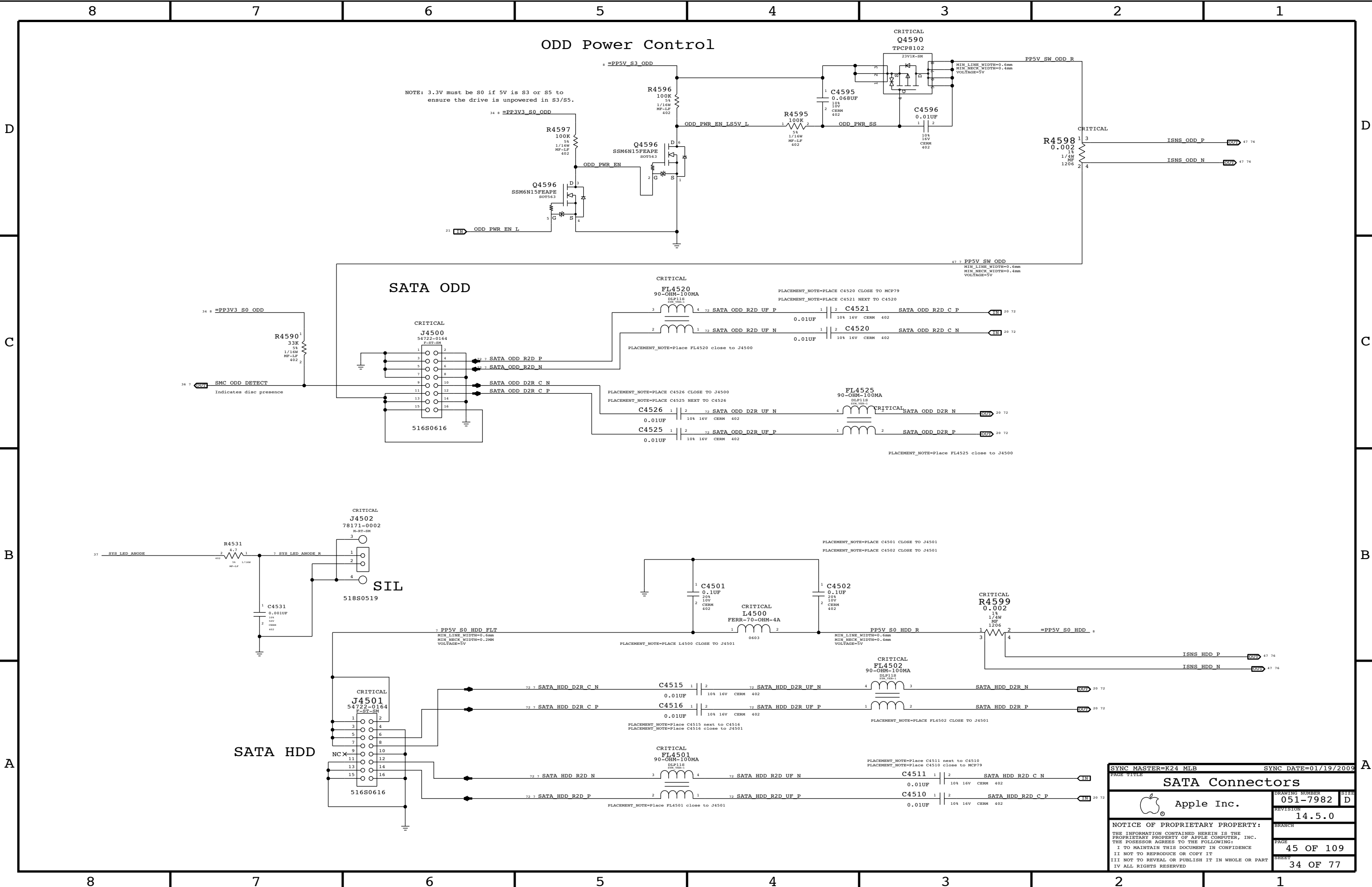
NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



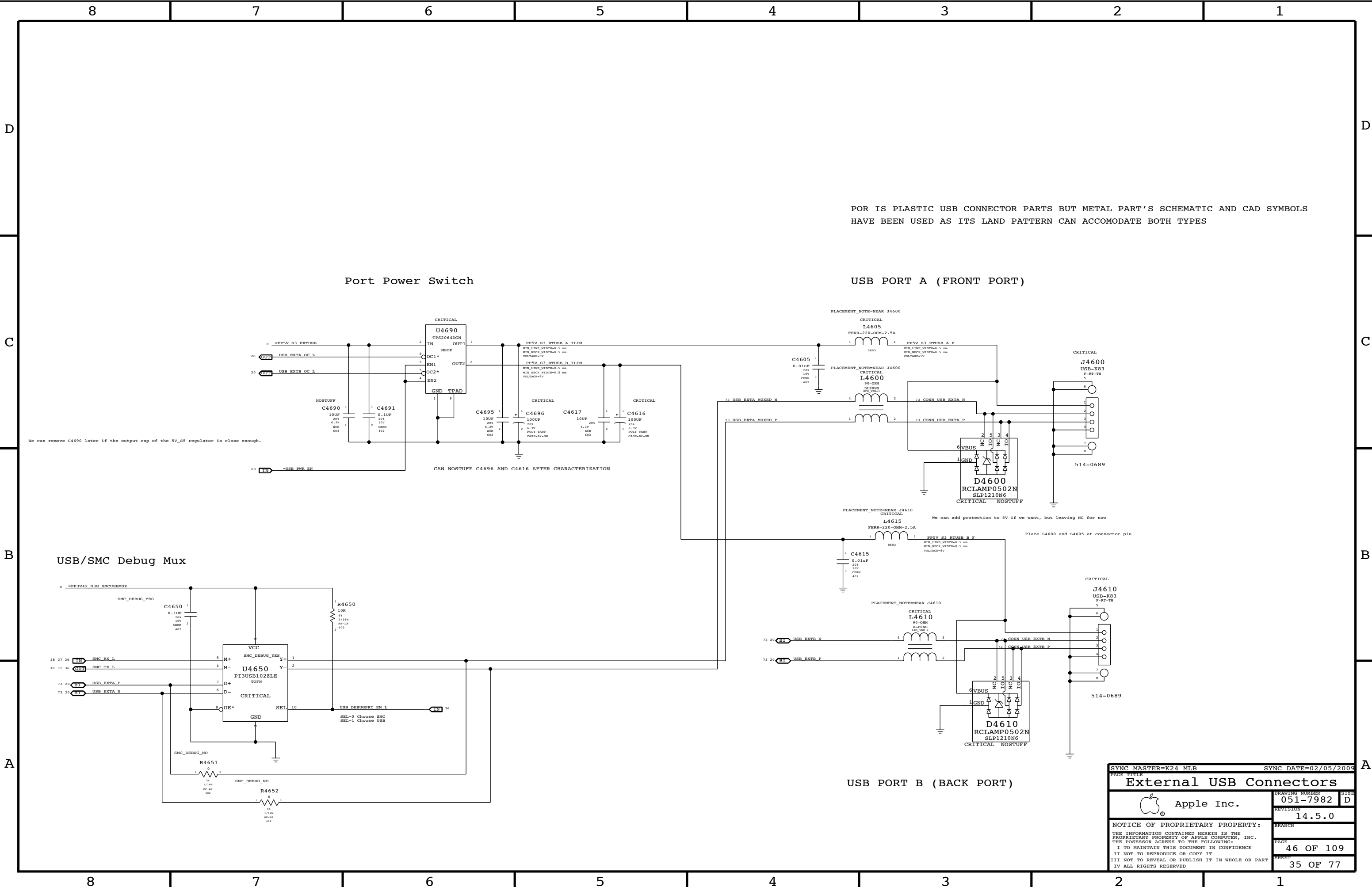
SYNC MASTER=K24 MLB		SYNC DATE=04/06/2009	
PAGE TITLE		Ethernet & AirPort Support	
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		PAGE	39 OF 109
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SYNC MASTER=K24 MLB		SYNC DATE=01/19/2009	
PAGE TITLE			
SATA Connectors		DRAWING NUMBER	051-7982
Apple Inc.		REVISION	14.5.0
		BRANCH	
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		SHEET	34 OF 77



POR IS PLASTIC USB CONNECTOR PARTS BUT METAL PART'S SCHEMATIC AND CAD SYMBOLS HAVE BEEN USED AS ITS LAND PATTERN CAN ACCOMODATE BOTH TYPES

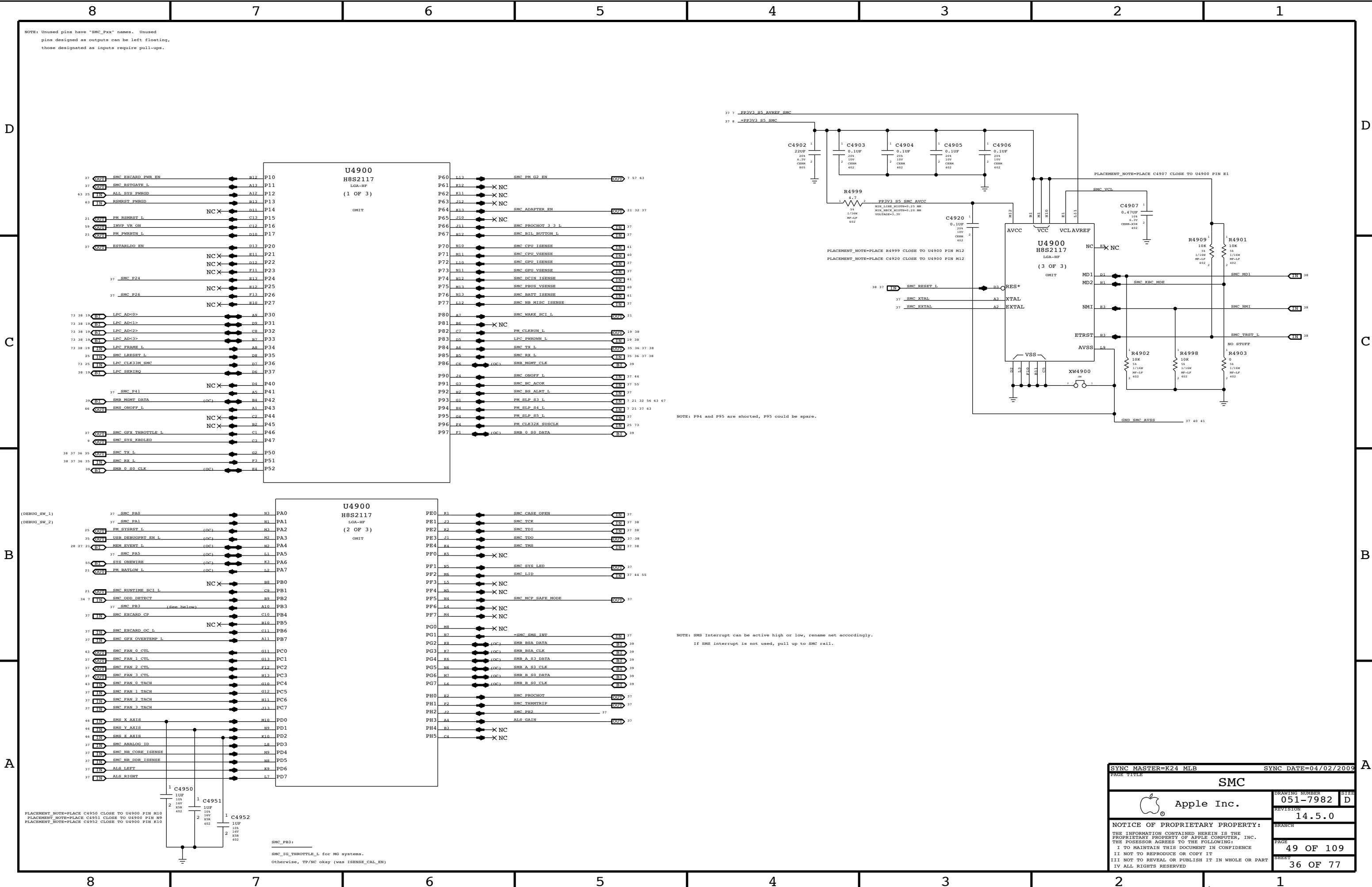
Port Power Switch

USB PORT A (FRONT PORT)

USB/SMC Debug Mux

USB PORT B (BACK PORT)

SYNC MASTER=K24 MLB		SYNC DATE=02/05/2009	
External USB Connectors		DRAWING NUMBER	051-7982
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		PAGE	46 OF 109
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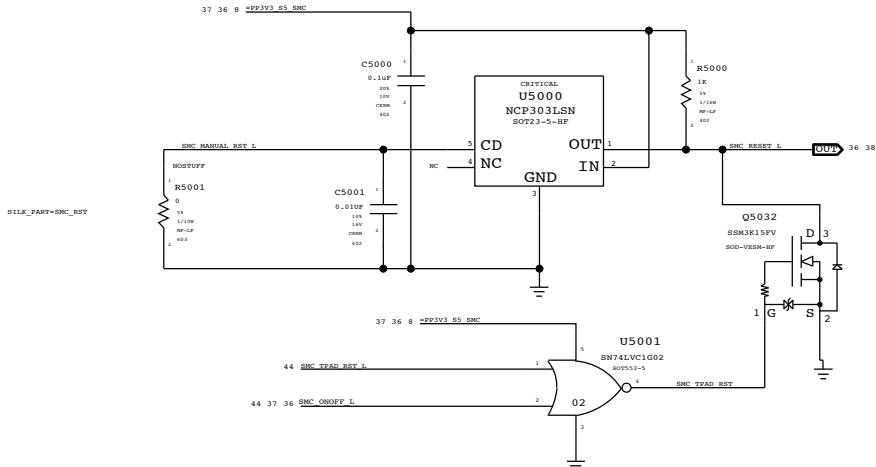
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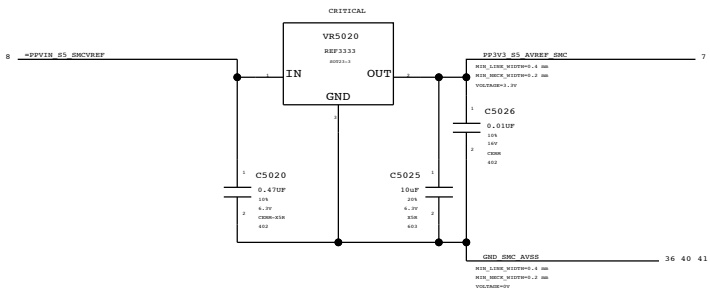
B

A

SMC Reset "Button" / Brownout Detect

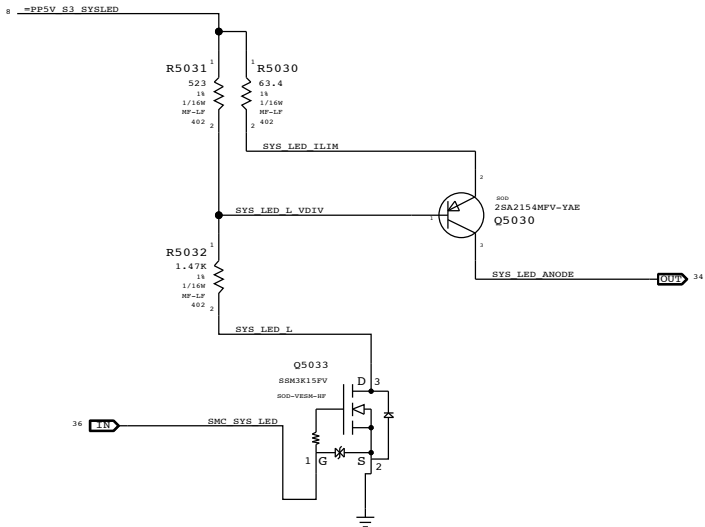


SMC AVREF Supply

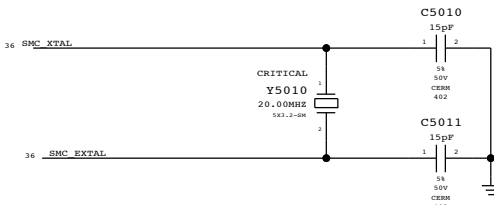


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35381381	35381912		ALL	ISL6002-31, INTERSIL

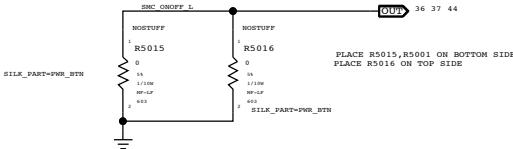
System (Sleep) LED Circuit



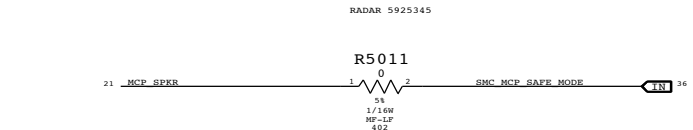
SMC Crystal Circuit



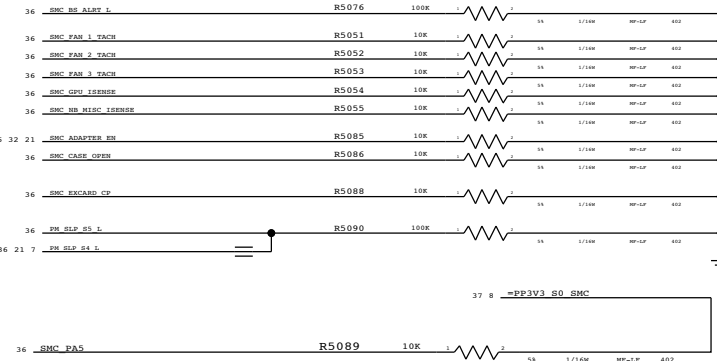
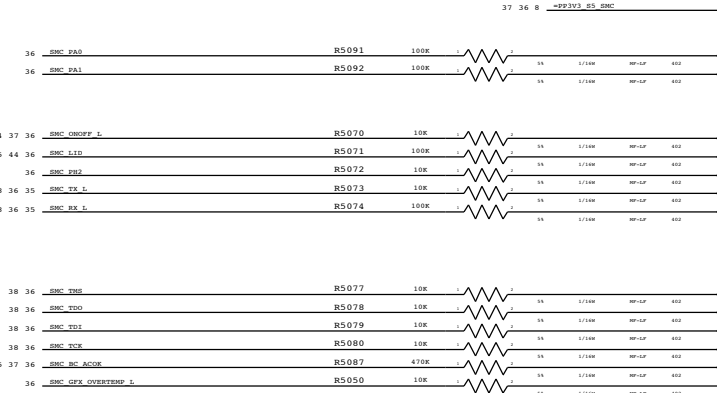
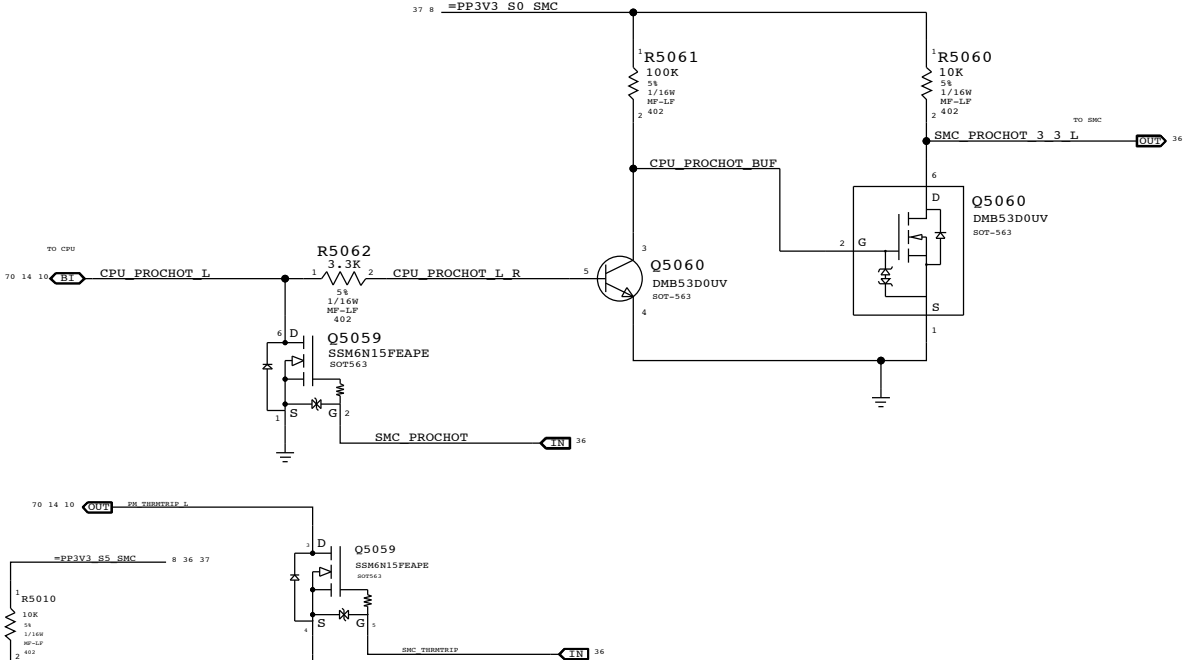
Debug Power "Button"



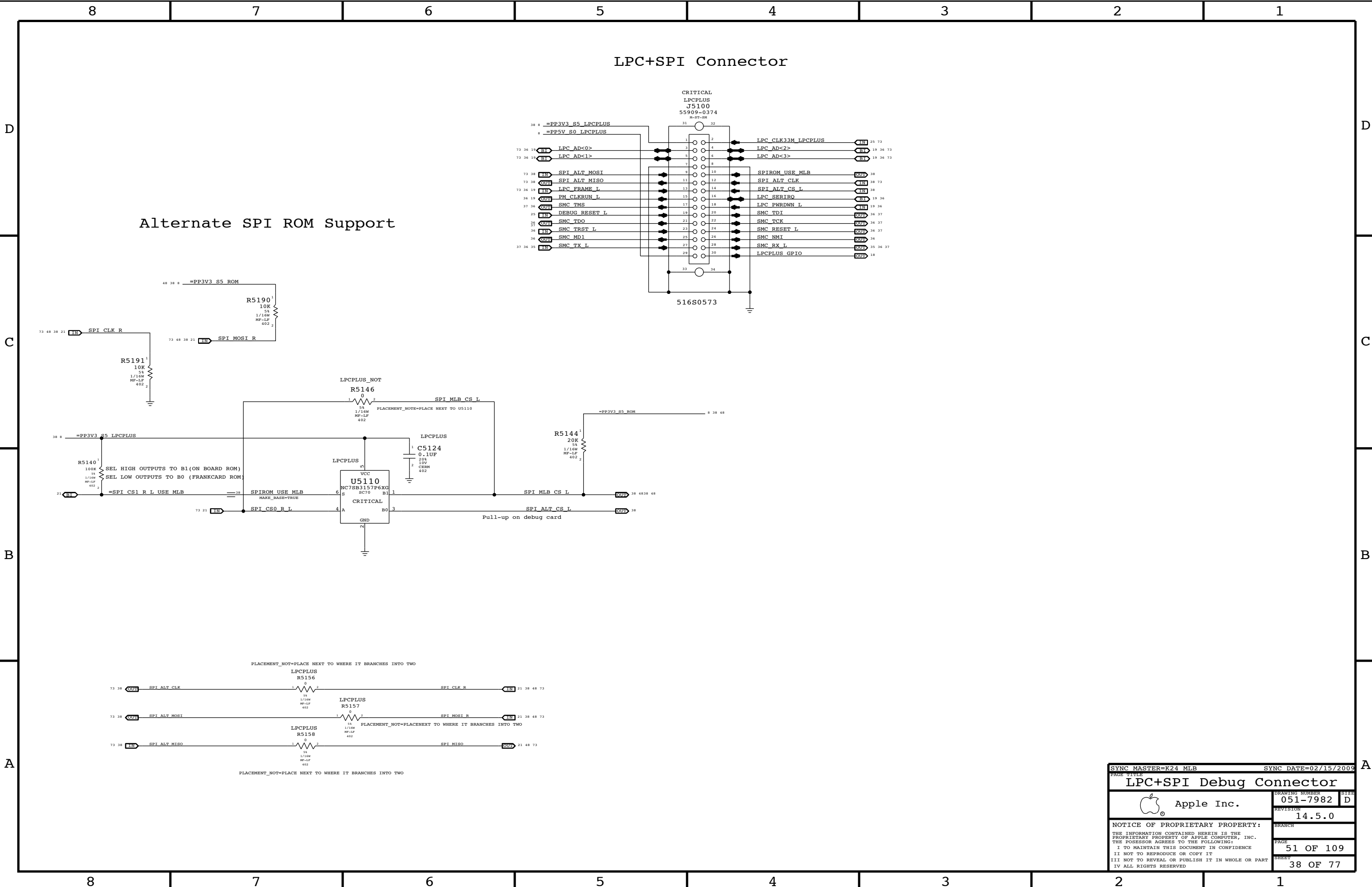
MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

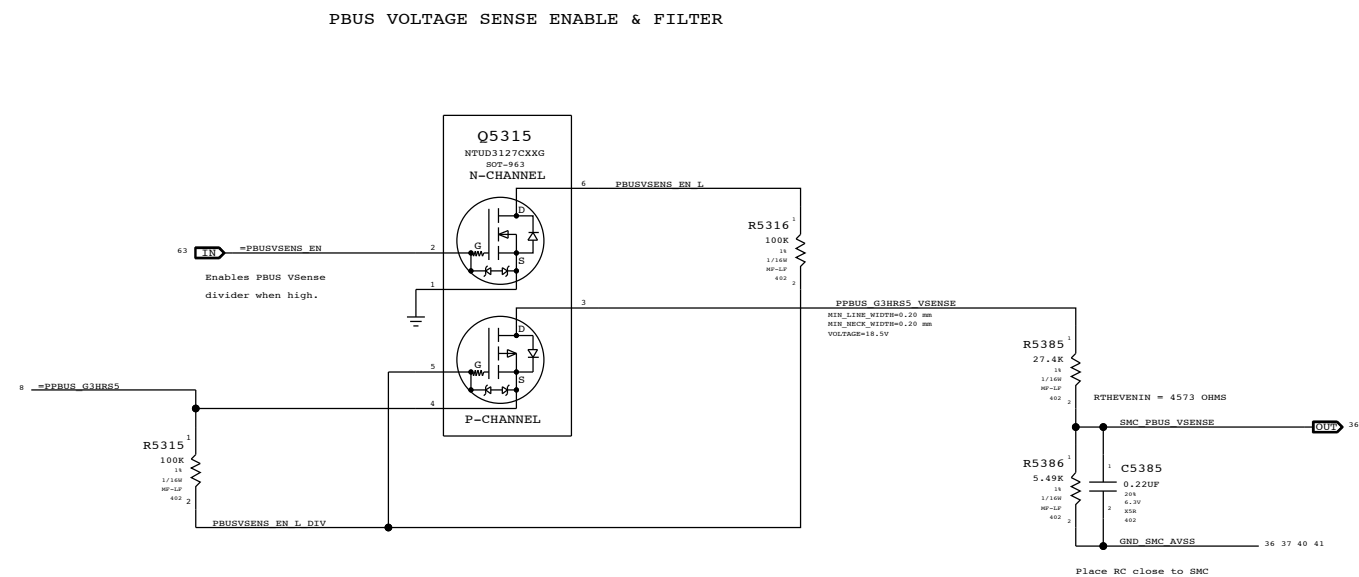
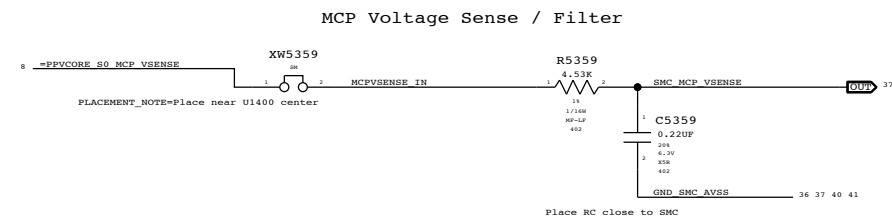
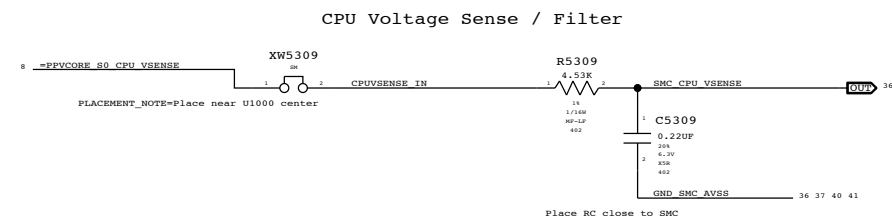


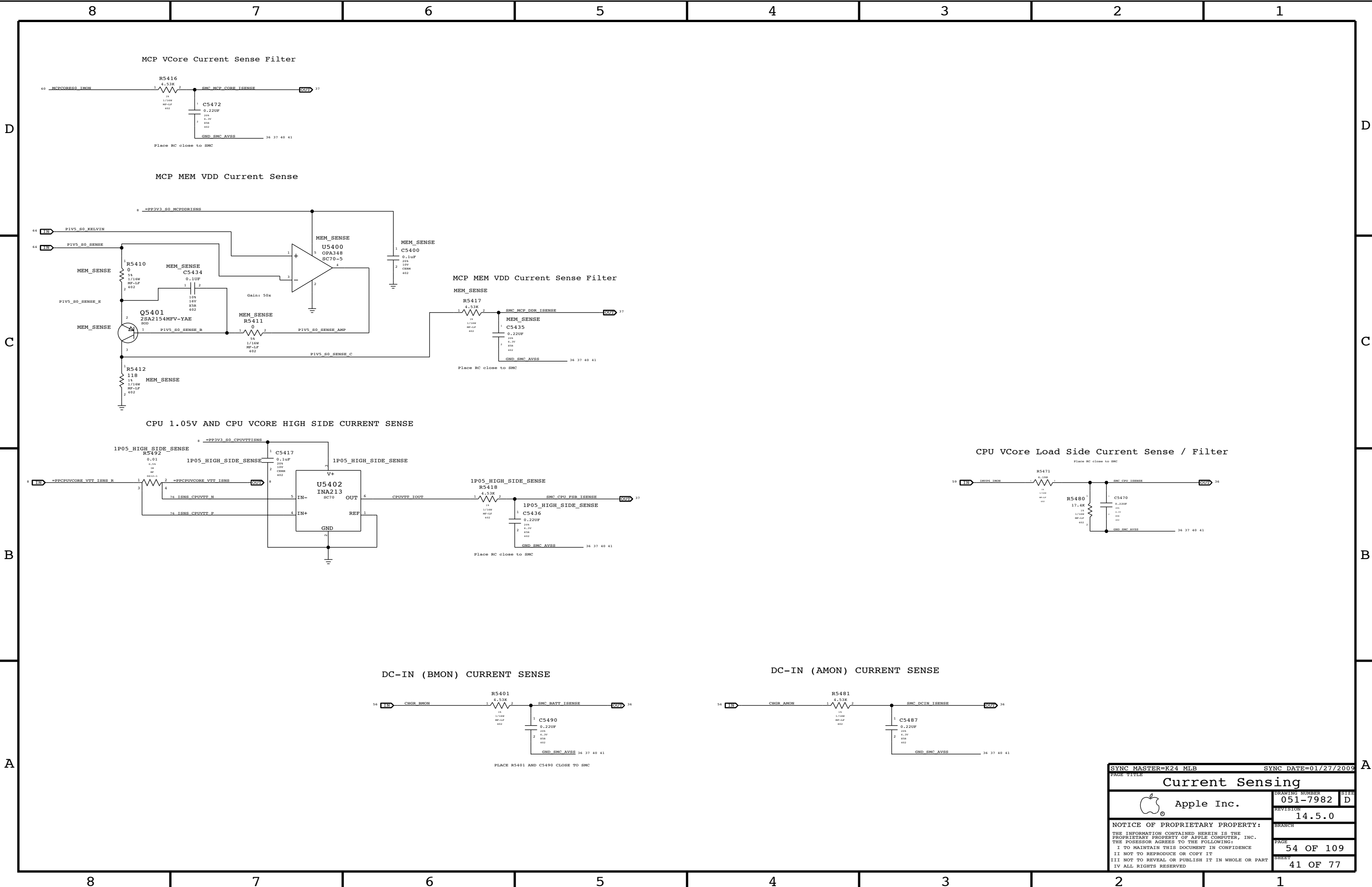
SMC FSB to 3.3V Level Shifting



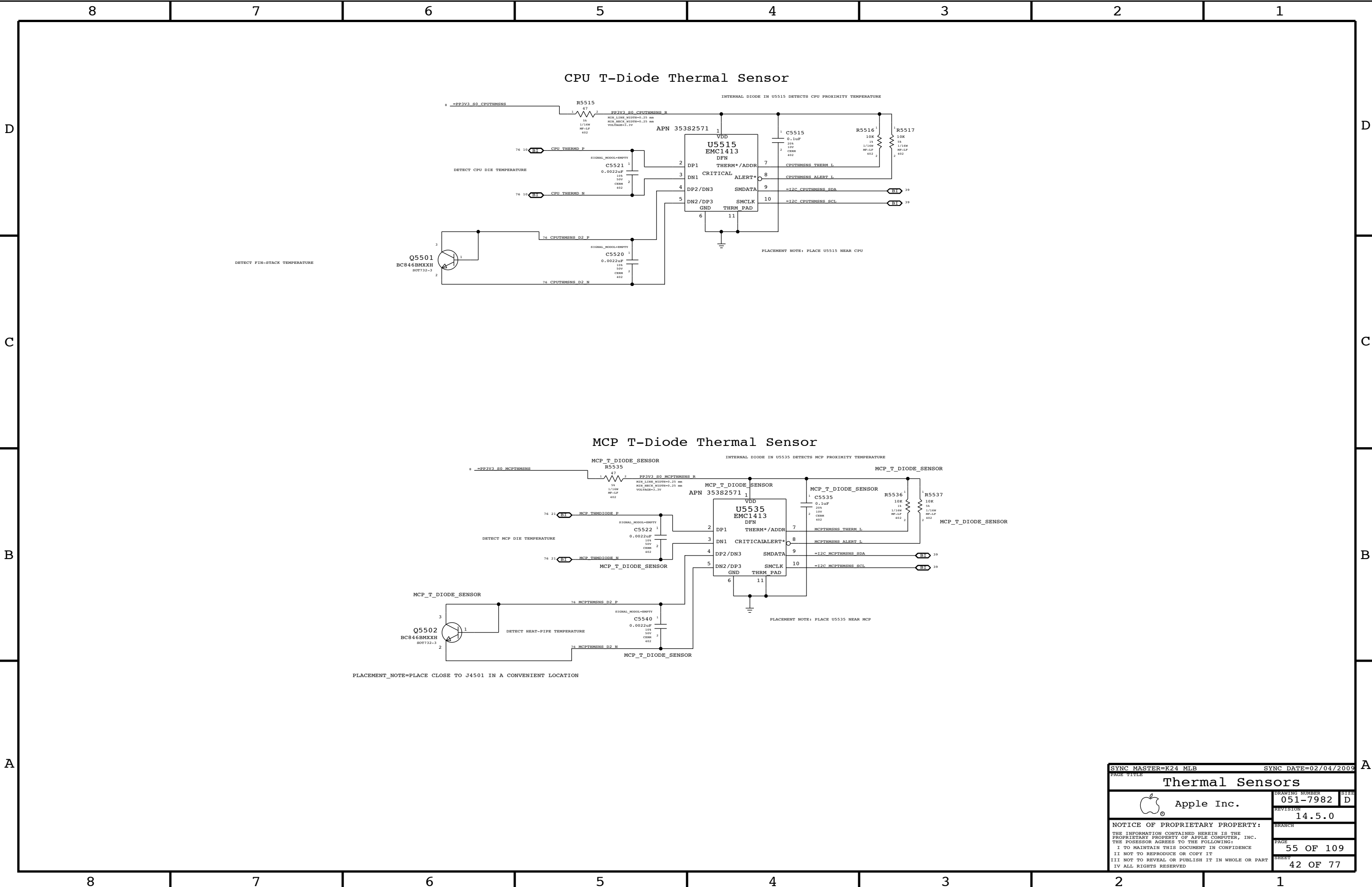
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PAGE TITLE		SMC Support	
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		REVISION	14.5.0
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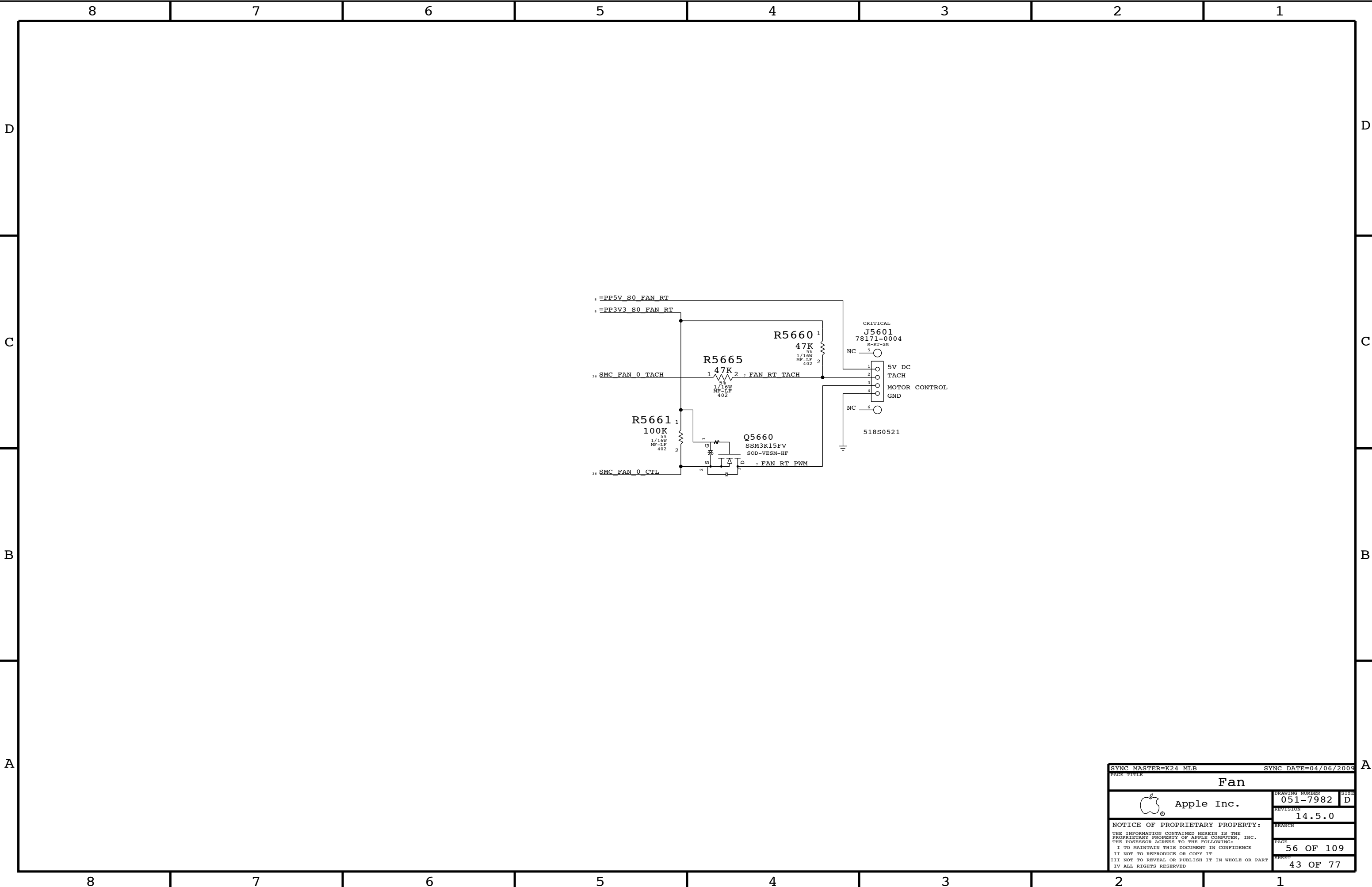


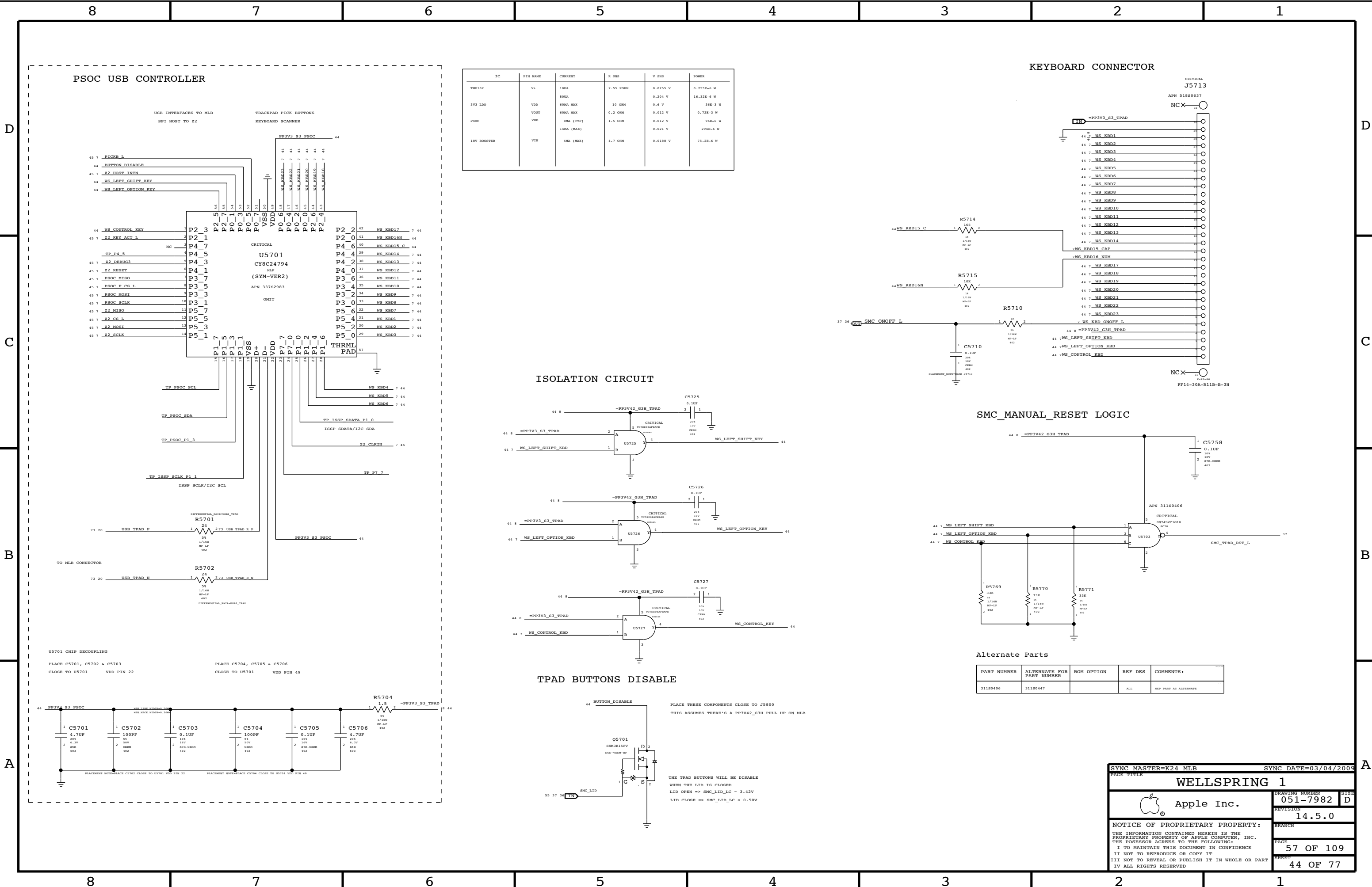




SYNC MASTER=K24 MLB		SYNC DATE=01/27/2009	
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Current Sensing			
 Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
		14.5.0	
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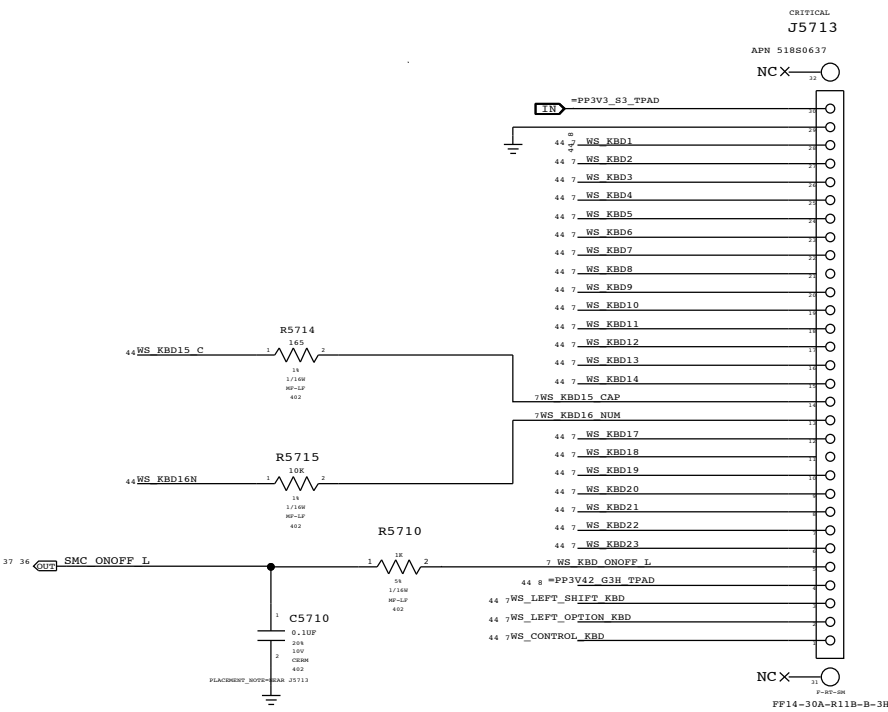




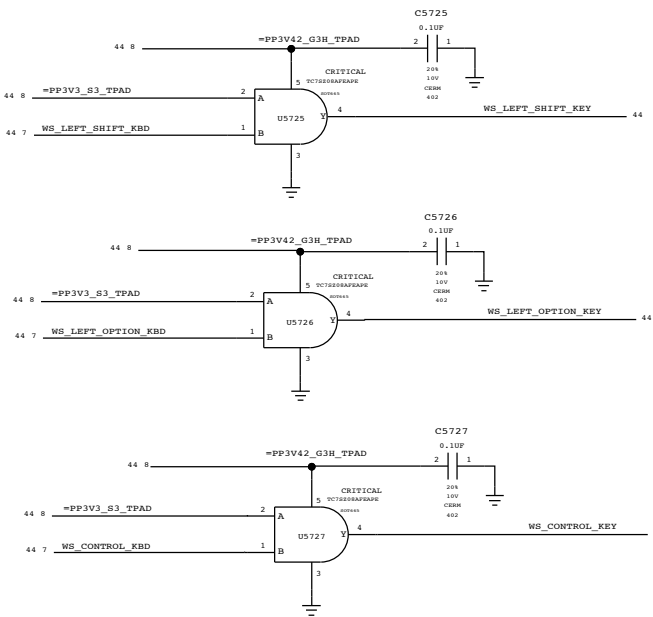


IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TPW102	V+	100A	2.55 KOHM	0.0255 V	0.255E-6 W
3V3 LDO	VDD	800A		0.204 V	16.32E-6 W
	VOUT	600A MAX	10 OHM	0.6 V	36E-3 W
PSoC	VDD	600A MAX	0.2 OHM	0.012 V	0.72E-3 W
		80A (TYP)	1.5 OHM	0.012 V	96E-6 W
		140A (MAX)		0.021 V	294E-6 W
1.8V BOOSTER	VIN	40A (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

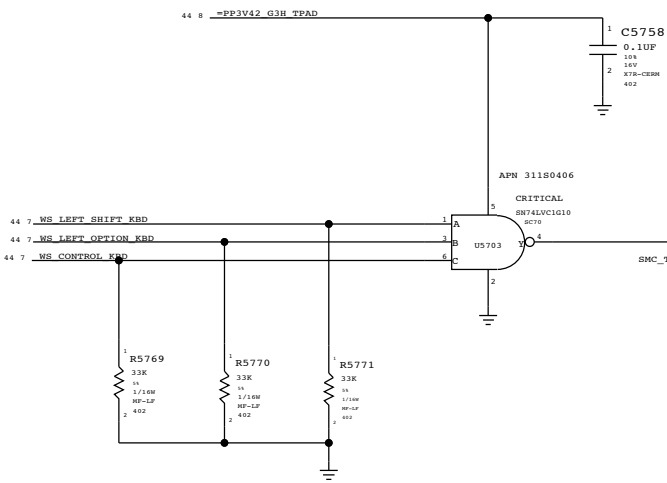
KEYBOARD CONNECTOR



ISOLATION CIRCUIT



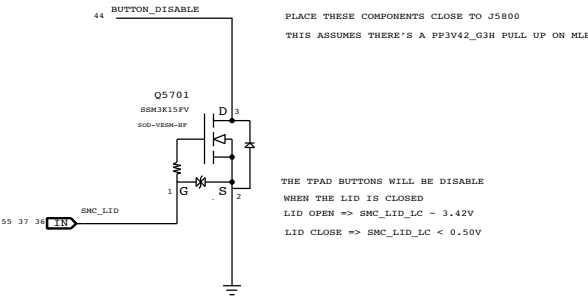
SMC_MANUAL_RESET LOGIC



Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
31150406	31150447		ALL	REV PART AS ALTERNATE

TPAD BUTTONS DISABLE



SYNC MASTER=K24 MLB

SYNC DATE=03/04/2009

WELLSPRING 1

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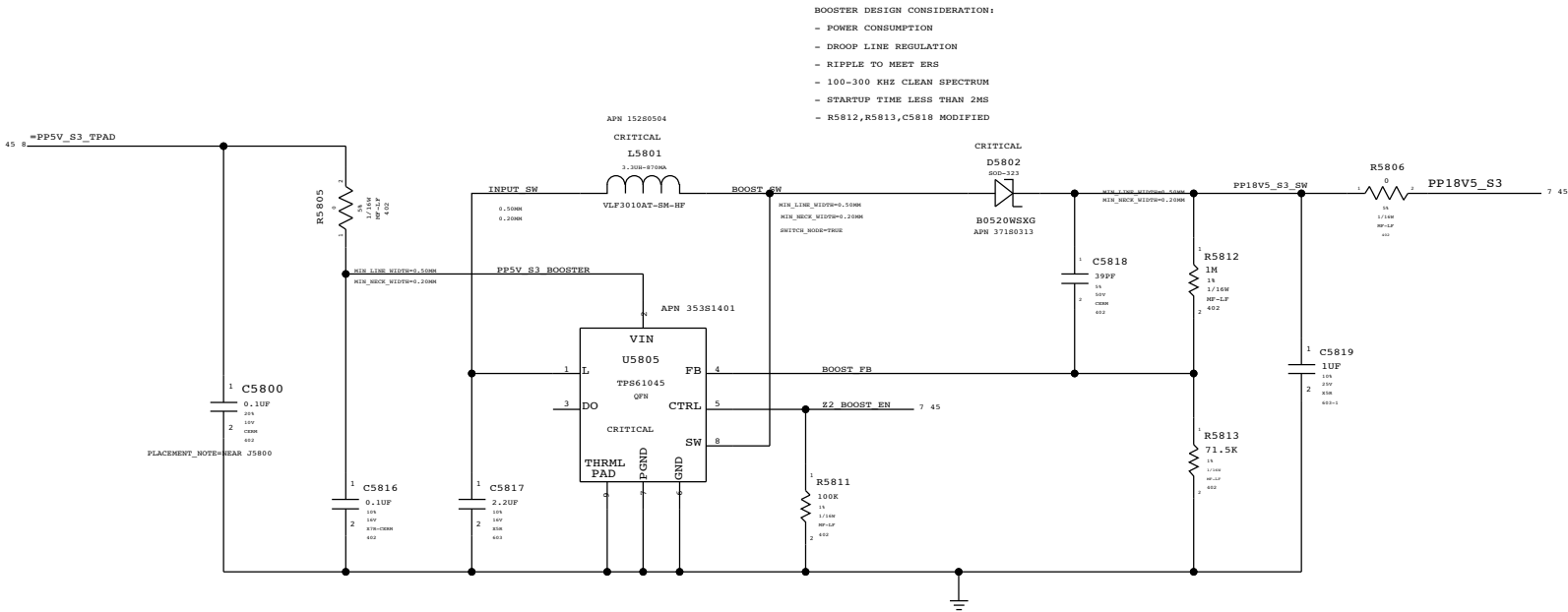
D

C

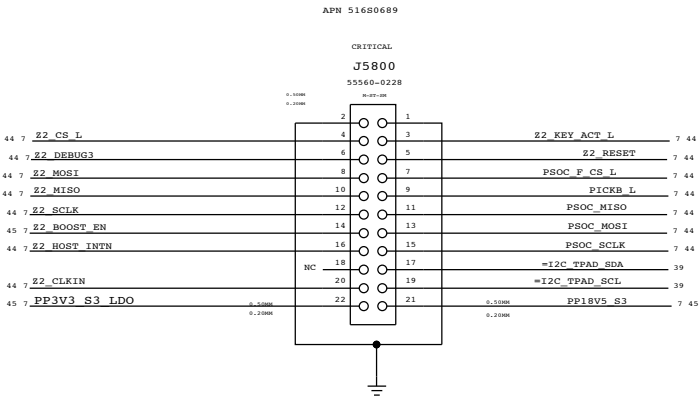
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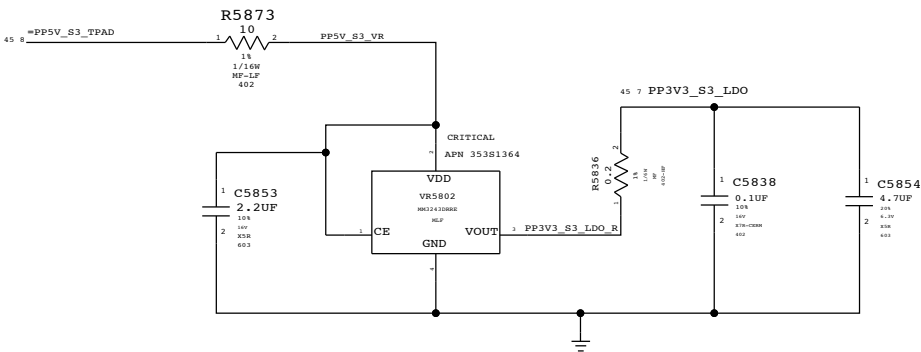
BOOSTER +18.5VDC FOR SENSORS

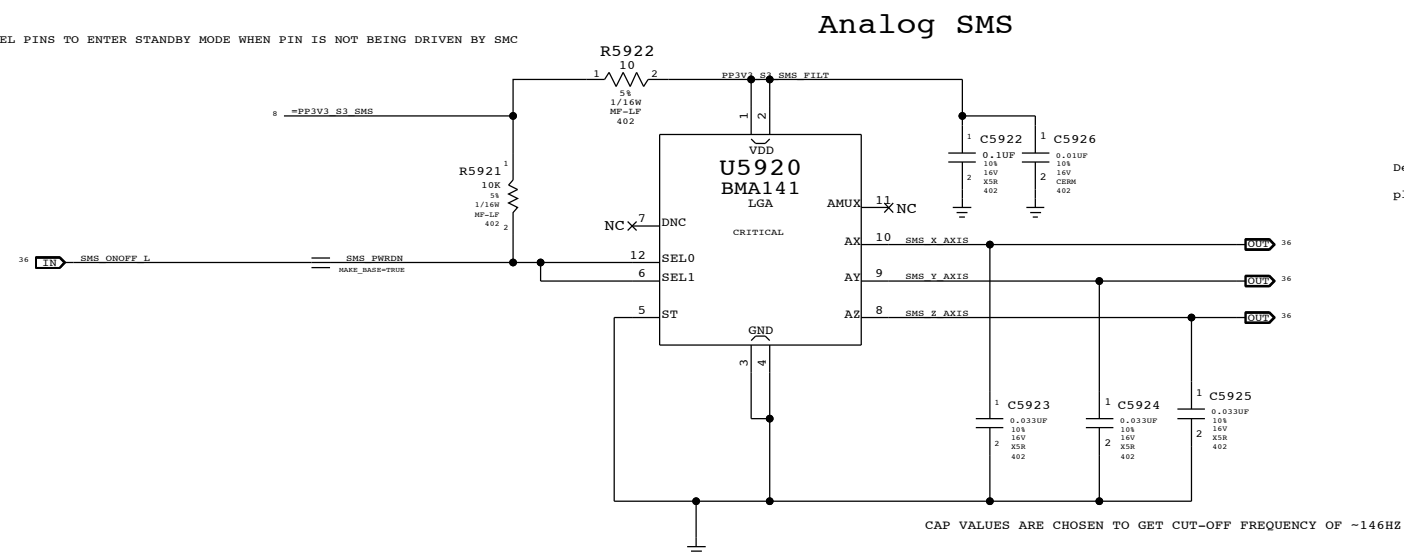
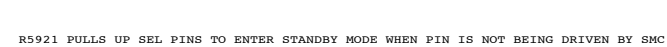


IPD FLEX CONNECTOR

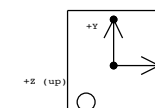


3V3 LDO FOR IPD





Desired orientation when
placed on board top-side:

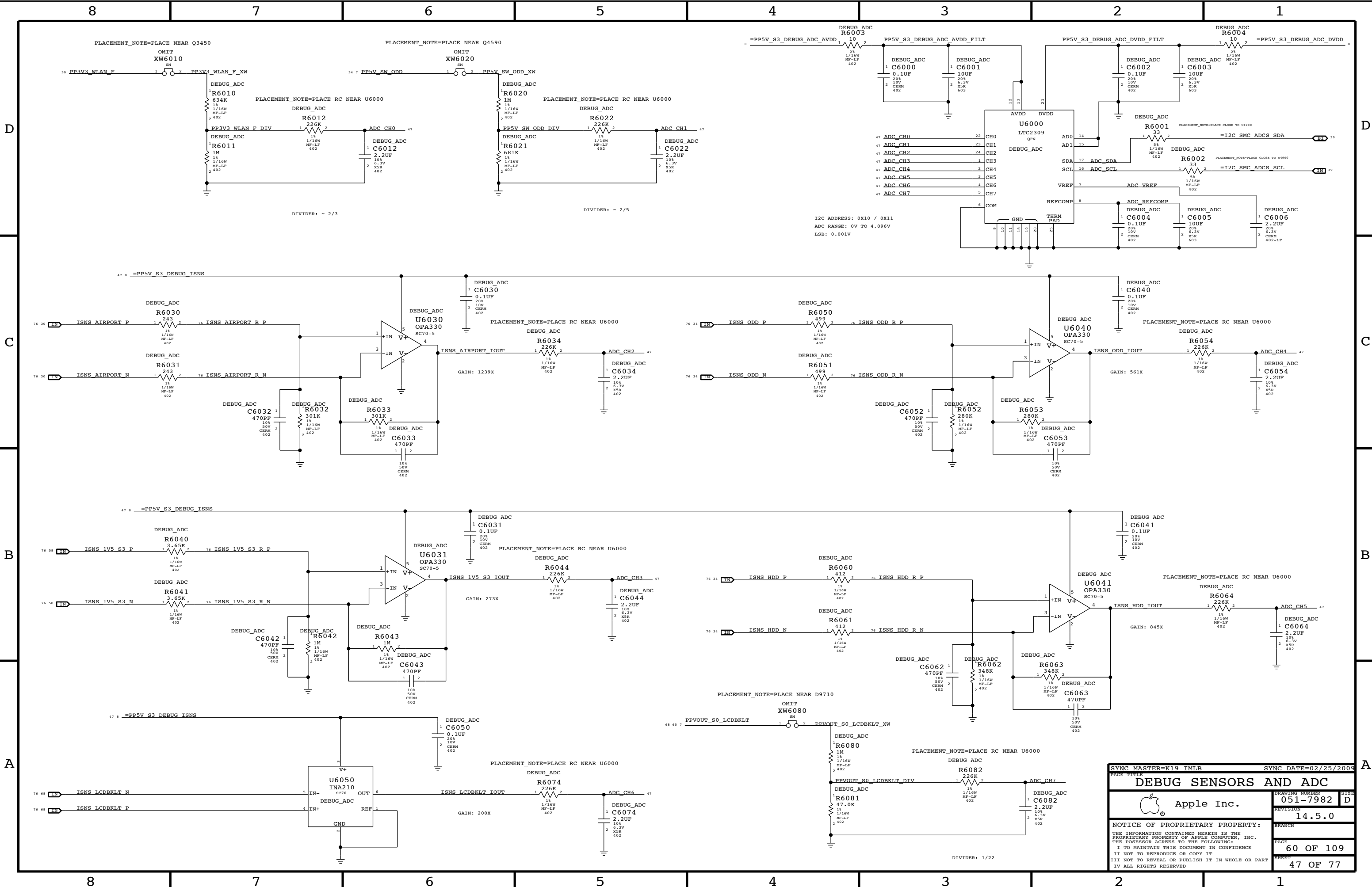


Front of system

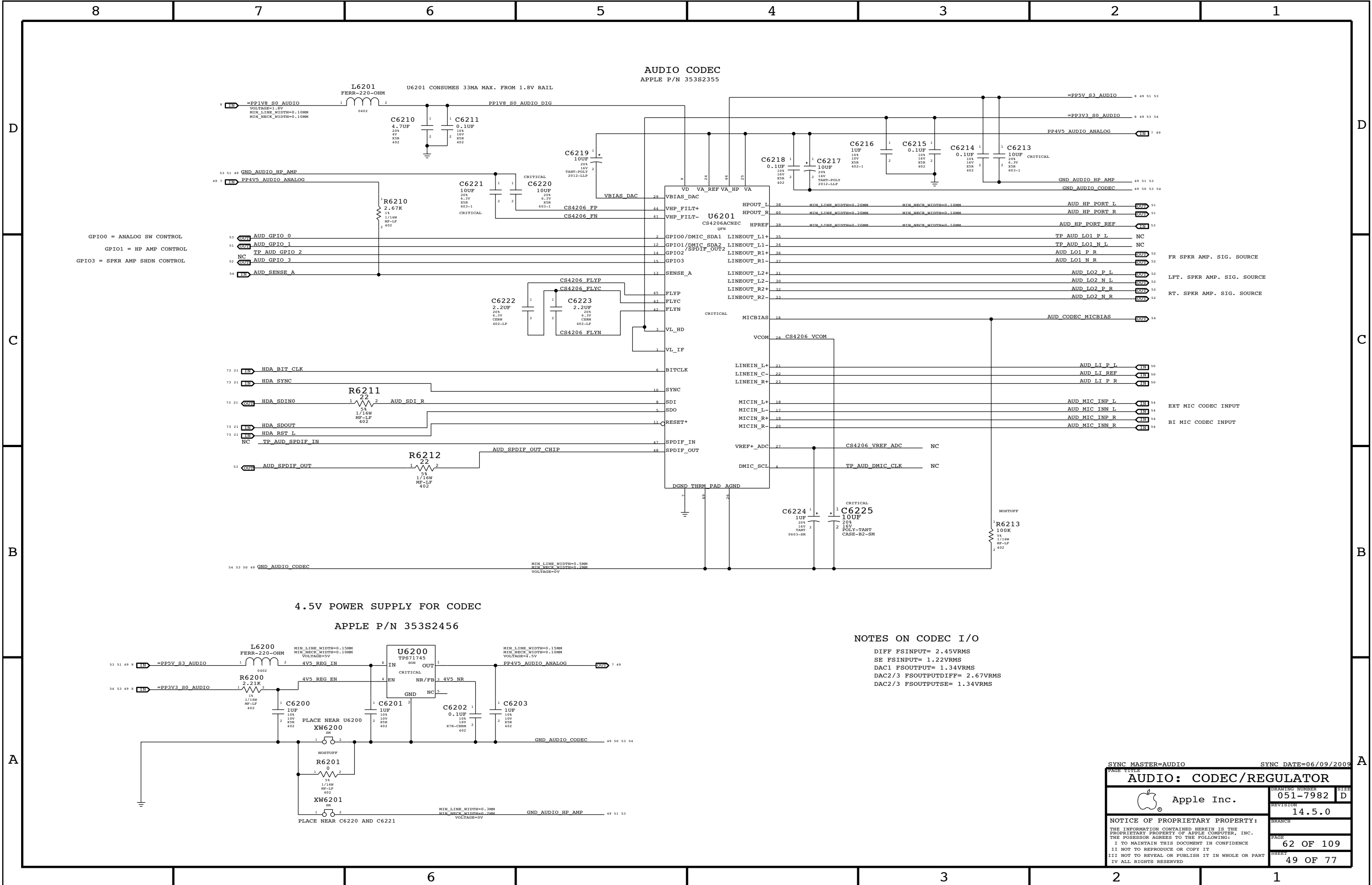
A diagram showing a downward-pointing arrow with a small circle at its base, indicating the front of a system.

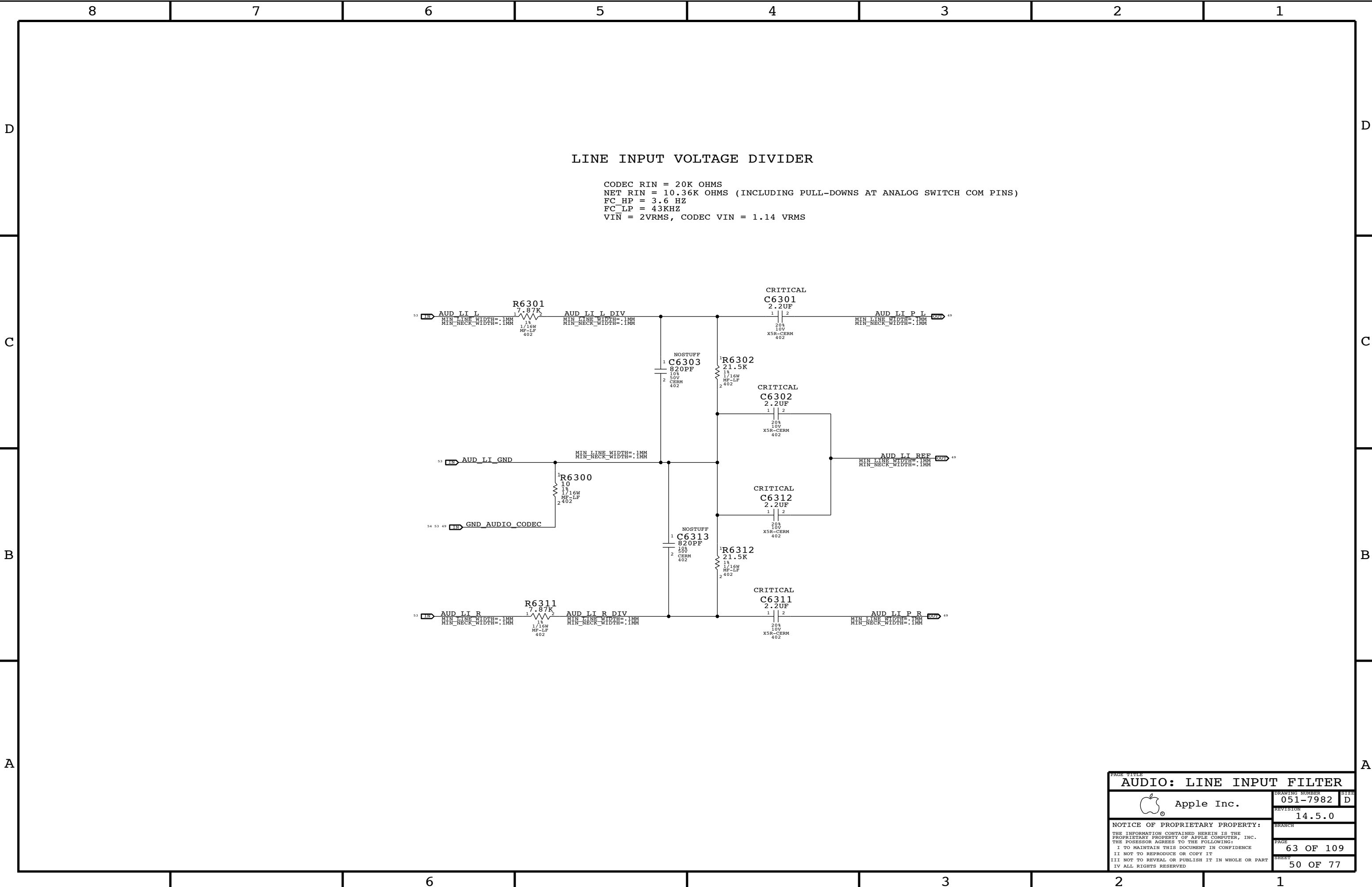
Circle indicates pin 1 location when placed
in correct orientation

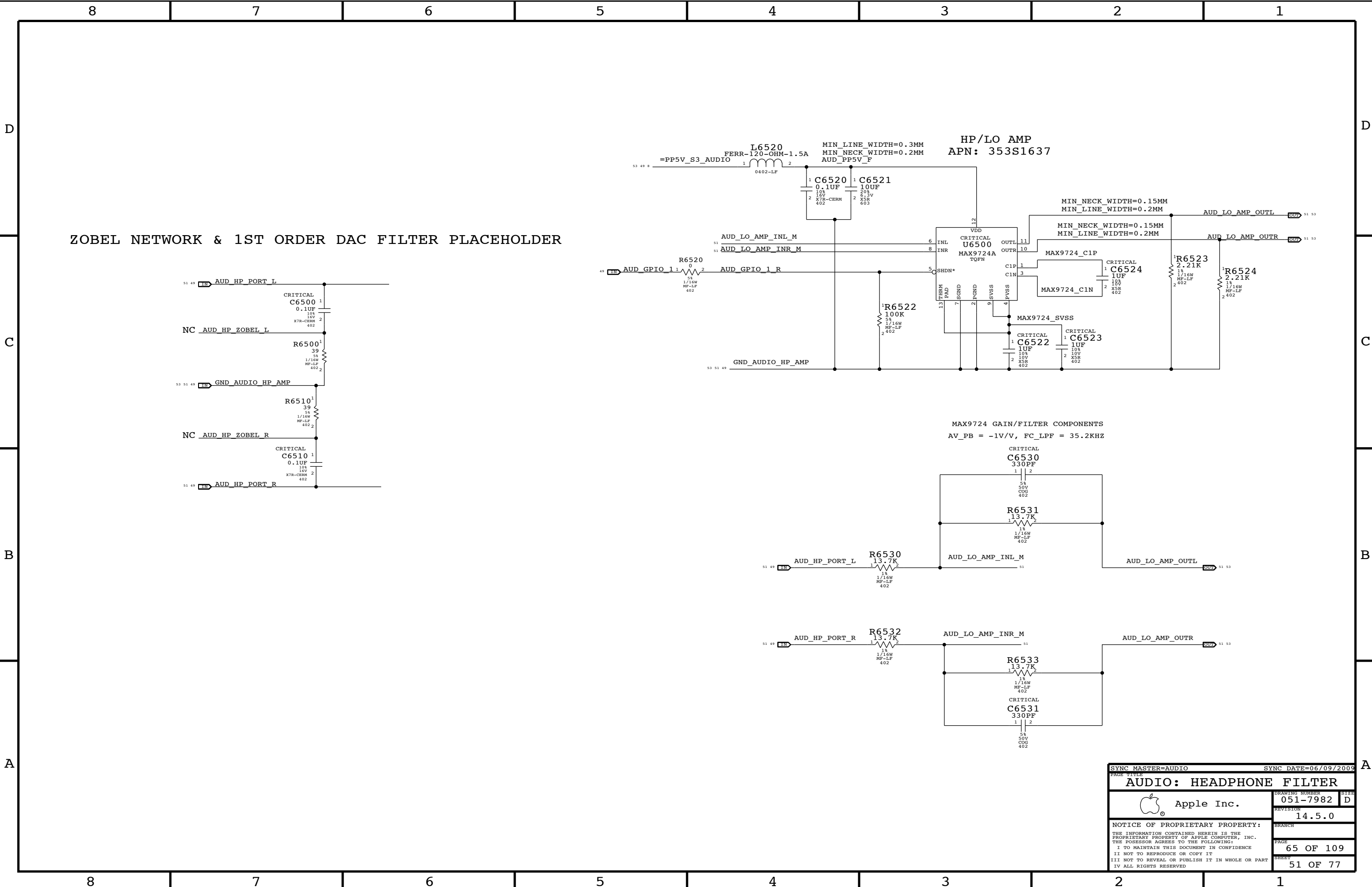
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SYNC MASTER=K19 IMLB		SYNC DATE=02/25/2009	
PAGE TITLE			
DEBUG SENSORS AND ADC			
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		SIZE	D
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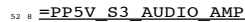




SYNC MASTER=AUDIO		SYNC DATE=06/09/2009	
PAGE TITLE			
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C



ALIAS OF PP5V_S3_REG, MIN_LINE WIDTH=0.60MM, MIN NECK WIDTH=0.20MM

52 8 =PP5V S3 AUDIO AMP



PAGE TITLE AUDIO: BREAKER AND

 Apple Inc.

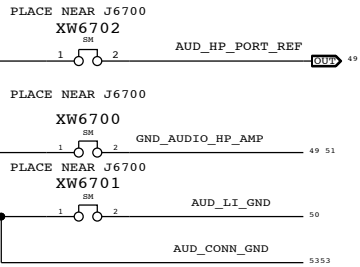
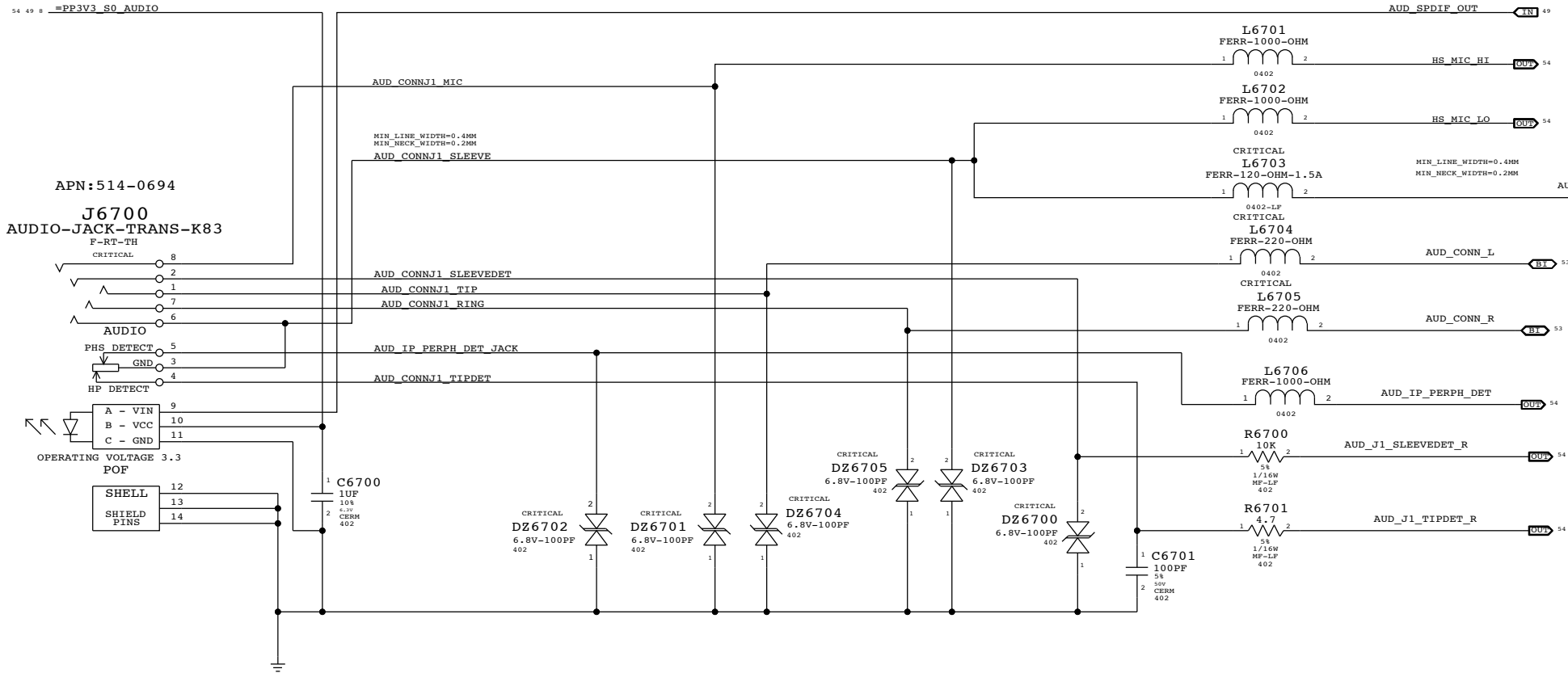
REVISION
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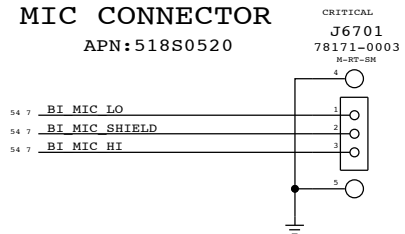
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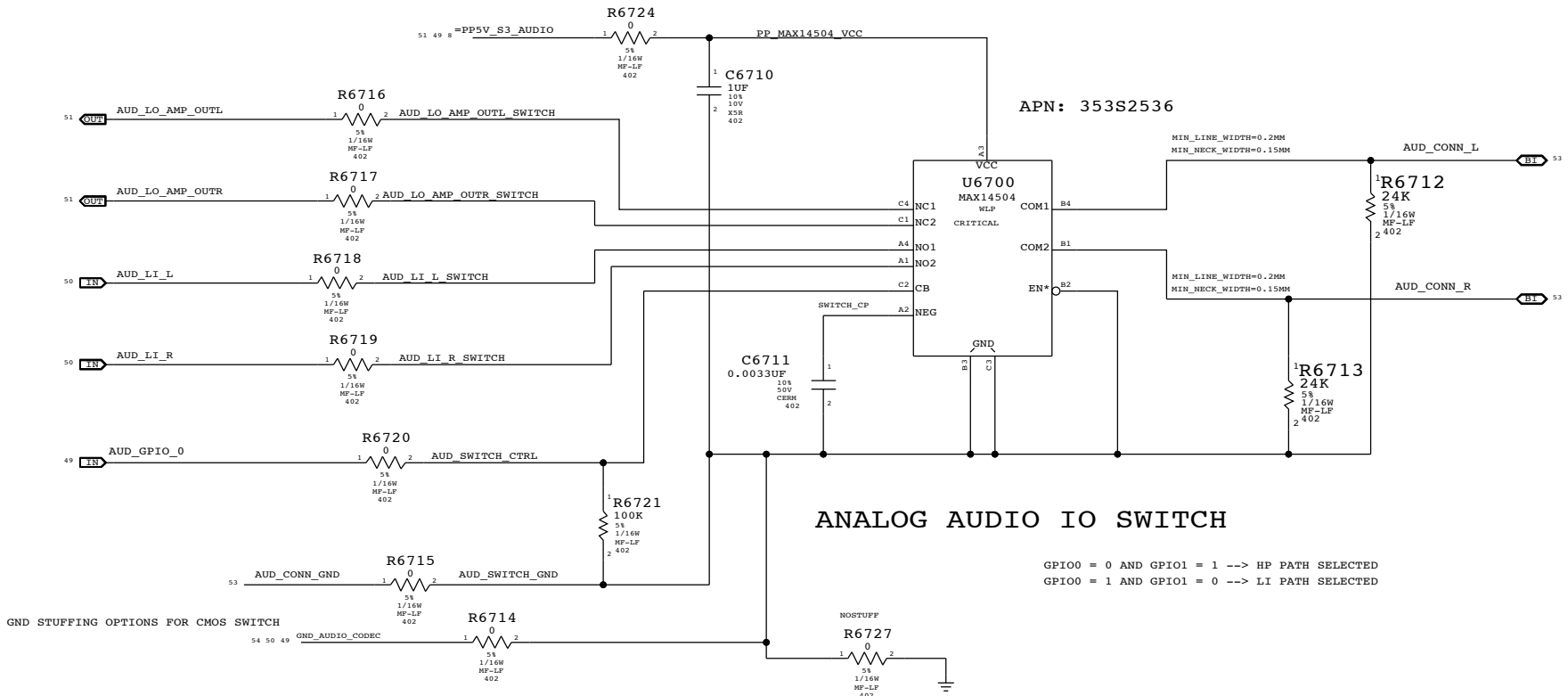
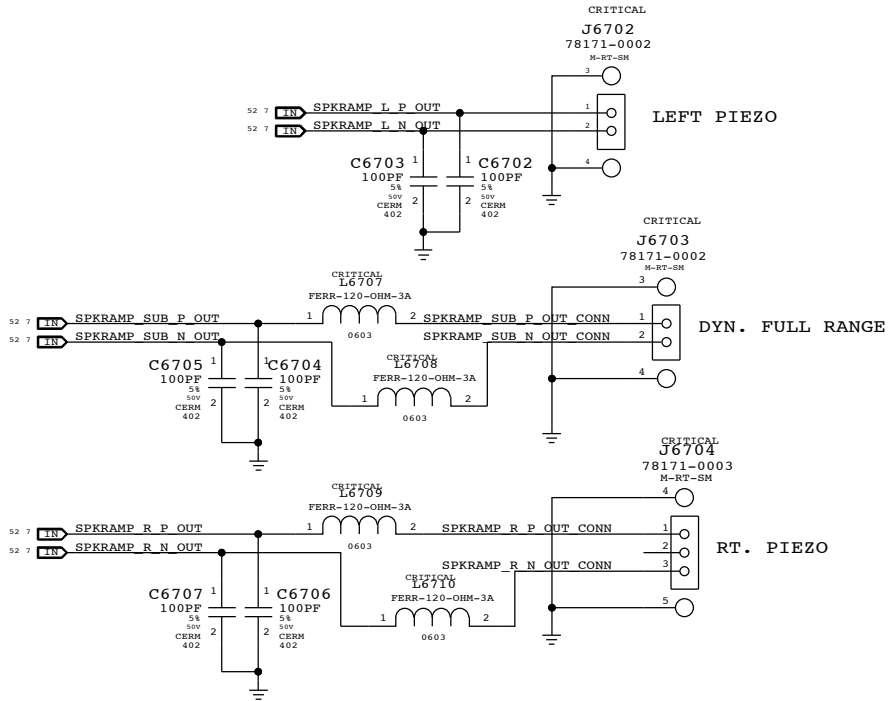
AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



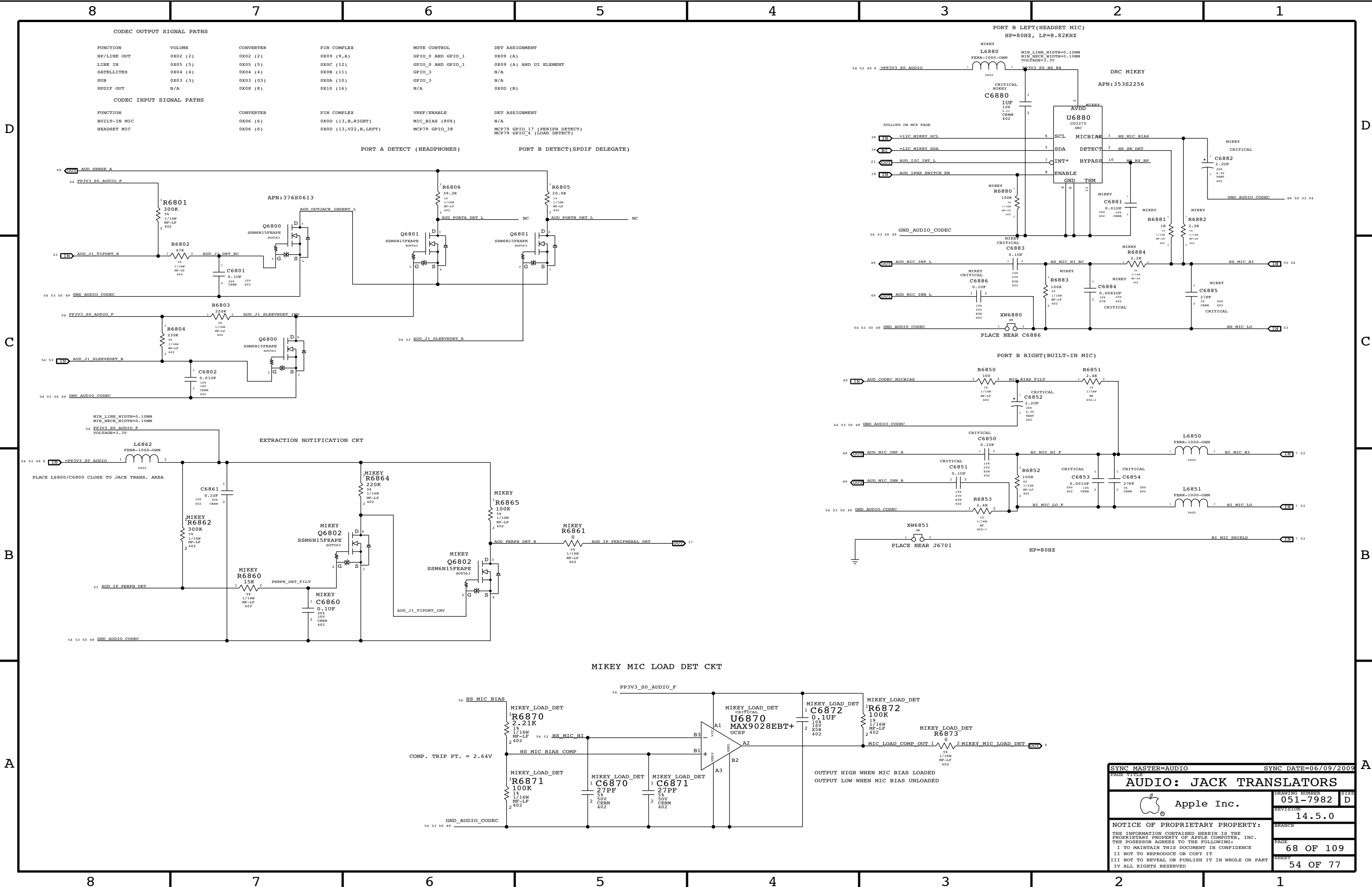
MIC CONNECTOR
APN:518S0520



SPEAKER CONNECTORS
APN:518S0519



SYNC MASTER=AUDIO		SYNC DATE=06/09/2009	
PAGE TITLE			
AUDIO: JACK			
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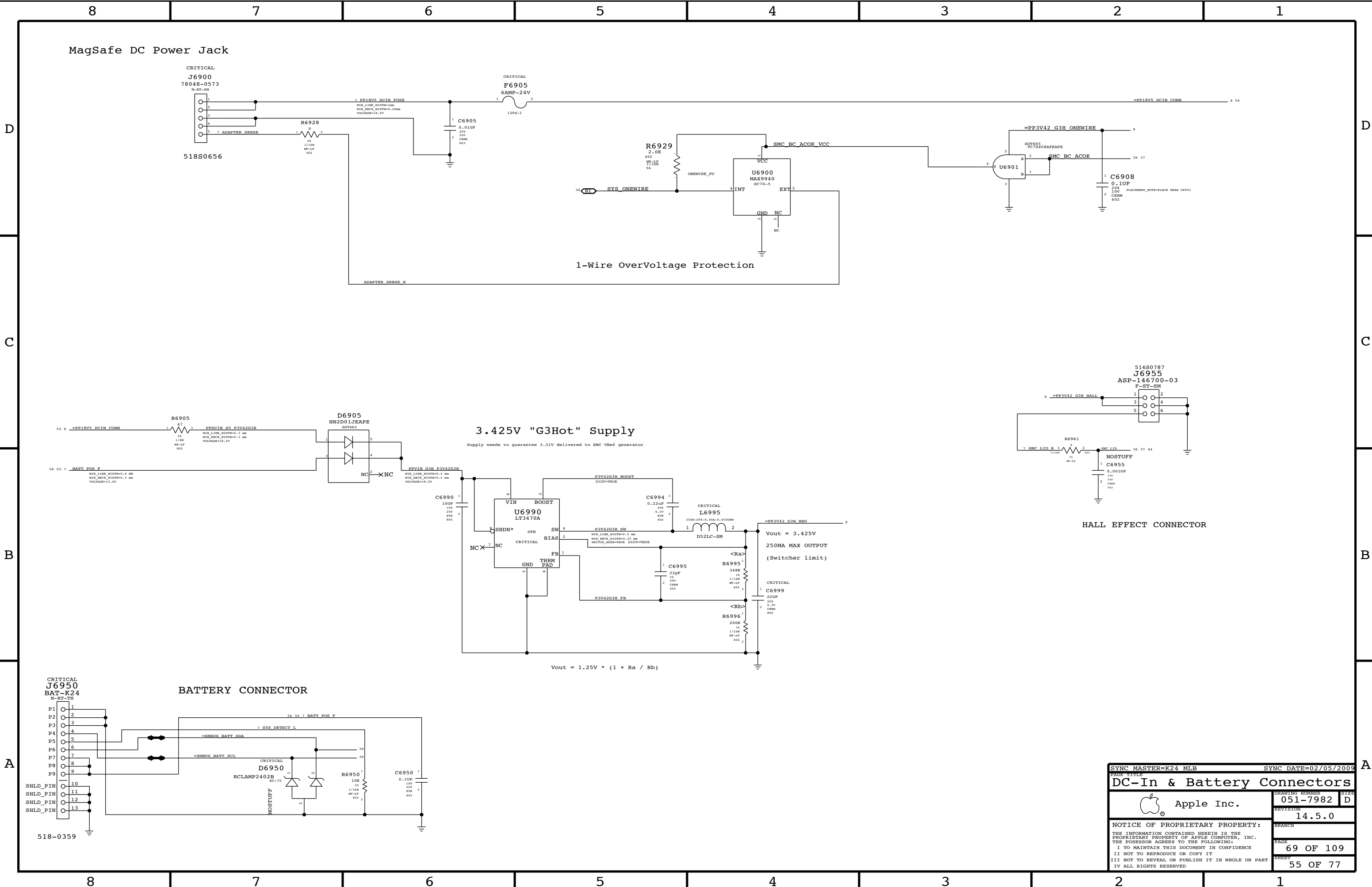
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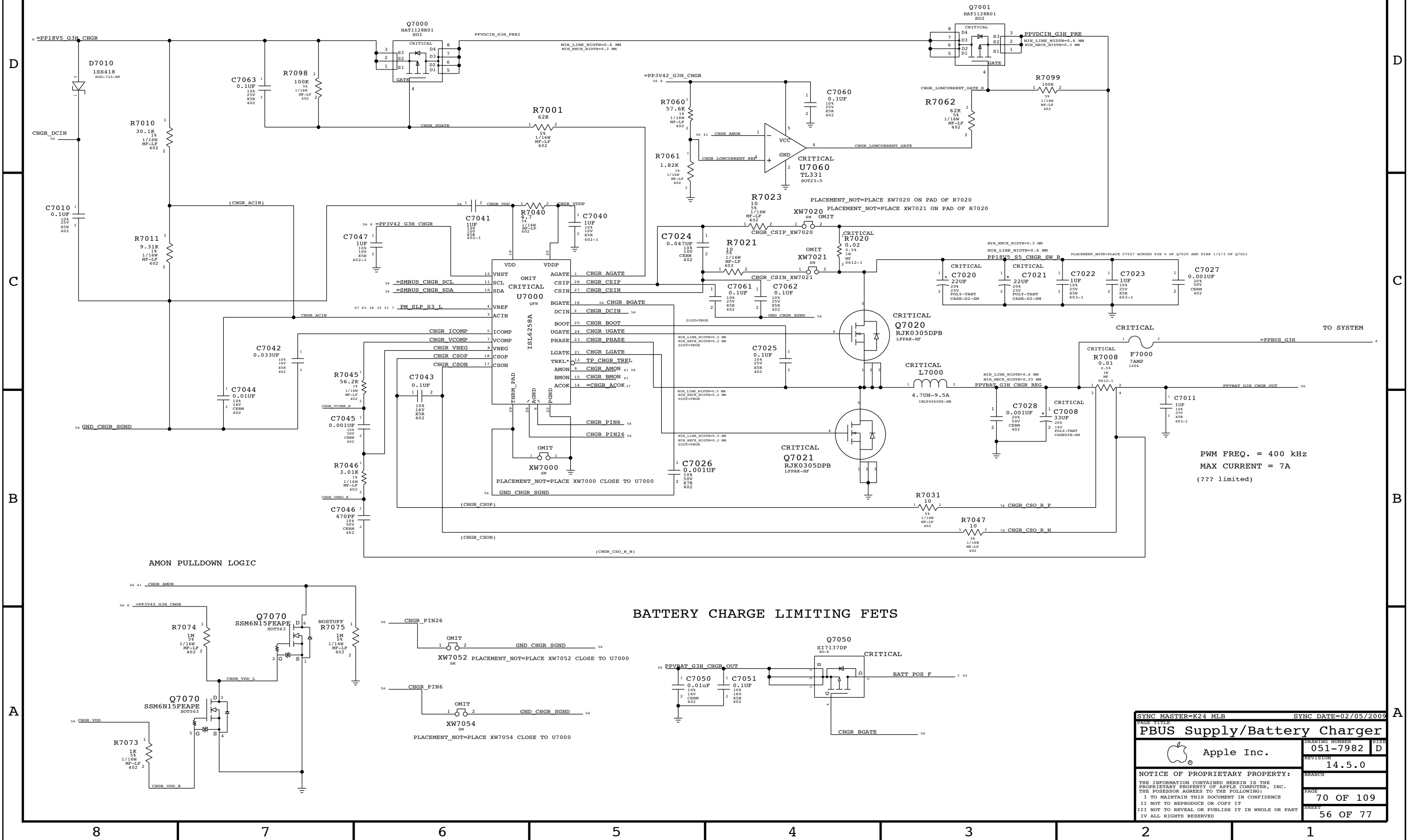
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PBUS SUPPLY / BATTERY CHARGER

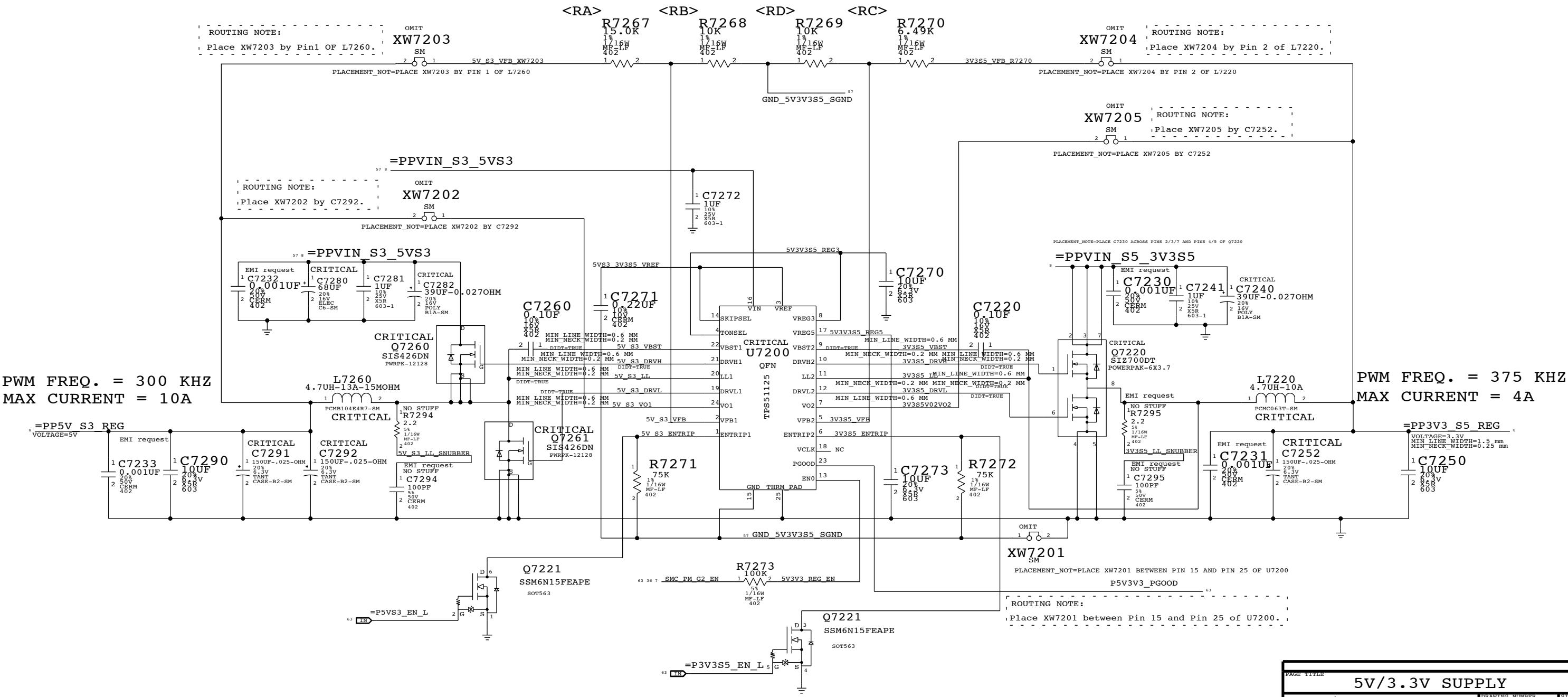


SYNC MASTER=K24 MLB		SYNC DATE=02/05/2009	
PAGE TITLE			
PBUS Supply/Battery Charger			
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5V S3/3.3V S5 POWER SUPPLY

$$VOUT = (2 * RA / RB) + 2$$

$$VOUT = (2 * RC / RD) + 2$$



SEPERATED MASTER PGOOD FOR BOTH 5V AND 3V3.

PAGE TITLE		
5V/3.3V SUPPLY		
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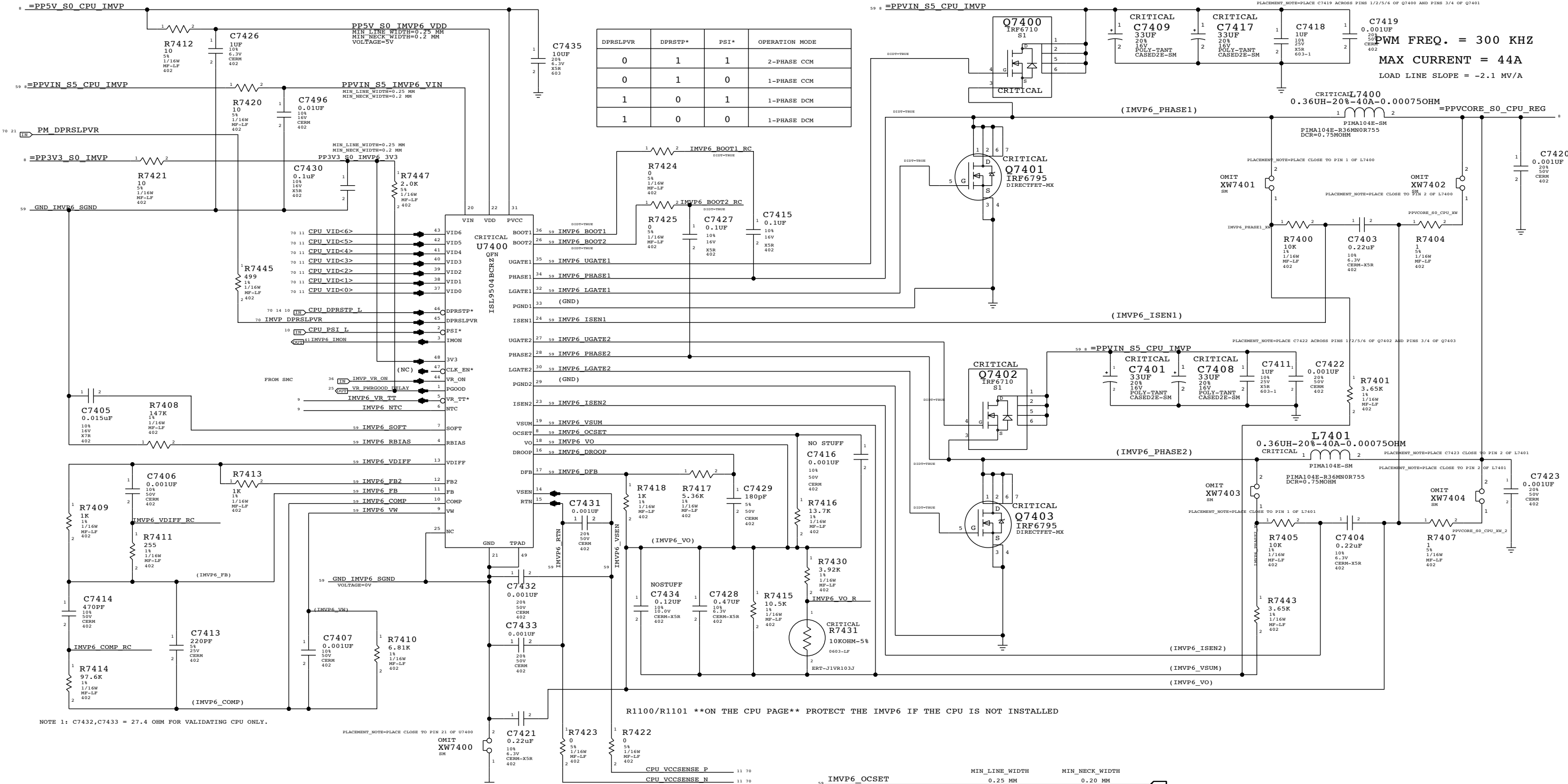
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IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6 PHASE1	1.5 MM	0.25 MM
IMVP6 BOOT1	0.25 MM	0.25 MM
IMVP6 UGATE1	1.5 MM	0.25 MM
IMVP6 LGATE1	1.5 MM	0.25 MM
IMVP6 ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6 PHASE2	0.25 MM	0.25 MM
IMVP6 BOOT2	0.25 MM	0.25 MM
IMVP6 UGATE2	0.25 MM	0.25 MM
IMVP6 LGATE2	0.25 MM	0.25 MM
IMVP6 ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6 OCSET	0.25 MM	0.20 MM
IMVP6 VSUM	0.25 MM	0.20 MM
GND IMVP6 SGND	0.50 MM	0.20 MM
IMVP6 VO	0.25 MM	0.20 MM
IMVP6 DROOP	0.25 MM	0.20 MM
IMVP6 DFB	0.25 MM	0.20 MM
IMVP6 SOFT	0.25 MM	0.20 MM
IMVP6 RBIAS	0.25 MM	0.20 MM
IMVP6 VDIFF	0.25 MM	0.20 MM
IMVP6 FB2	0.25 MM	0.20 MM
IMVP6 FB	0.25 MM	0.20 MM
IMVP6 COMP	0.25 MM	0.20 MM
IMVP6 VW	0.25 MM	0.25 MM
IMVP6 RTN	0.25 MM	0.25 MM
IMVP6 VSEN	0.25 MM	0.25 MM

SYNC MASTER=K24 MLB

SYNC DATE=03/03/2009

IMVP6 CPU VCore Regulator

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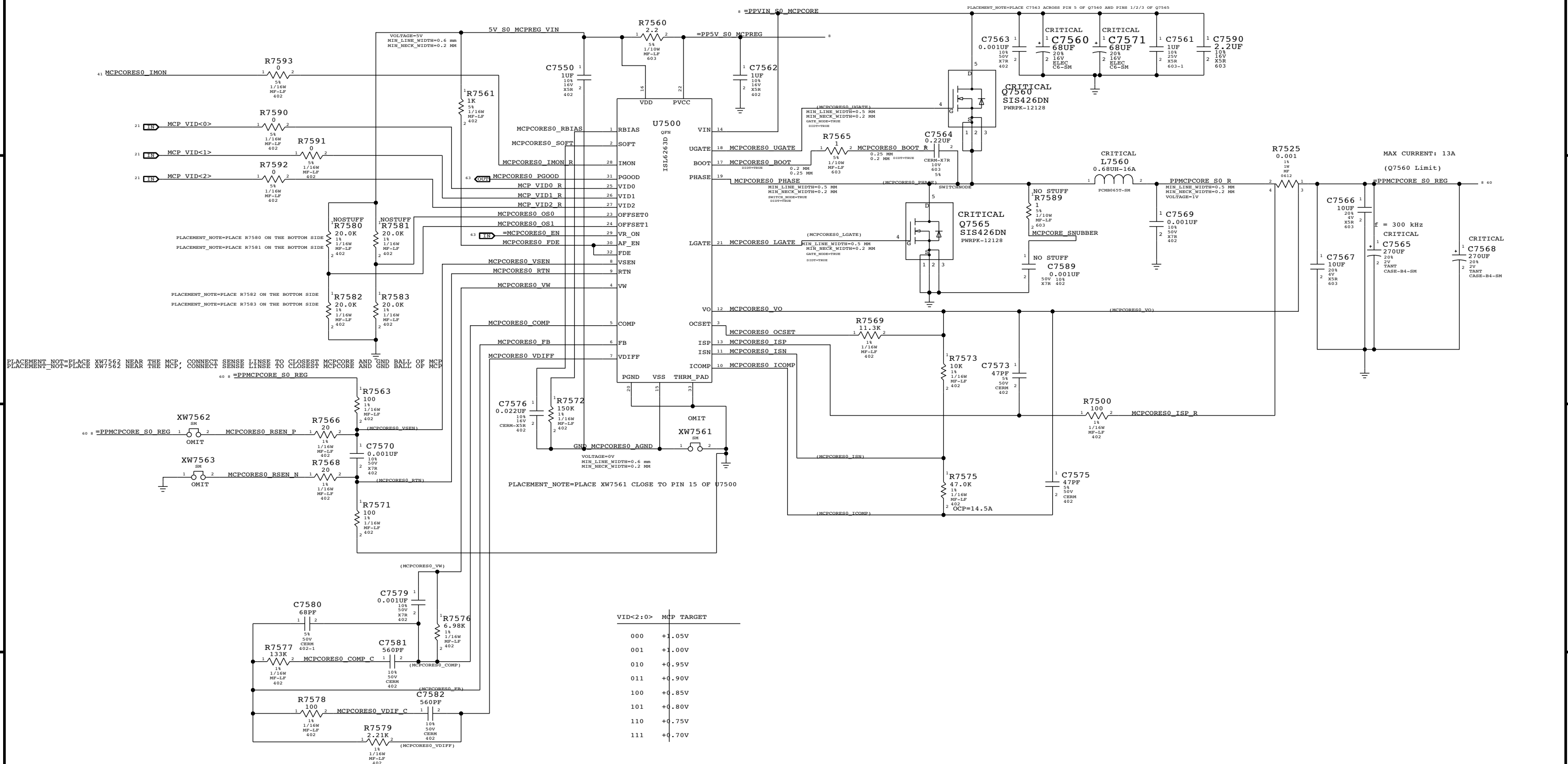
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SYNC MASTER=K24 MLB

SYNC DATE=02/15/2009

MCP CORE REGULATOR

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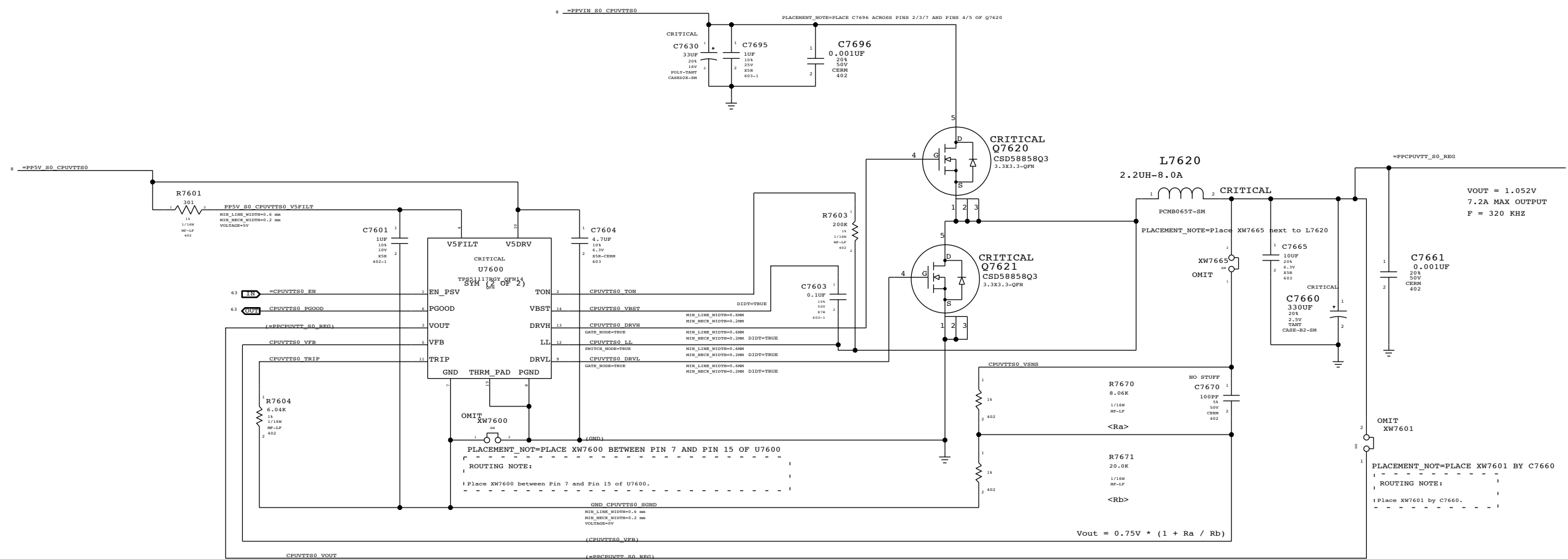
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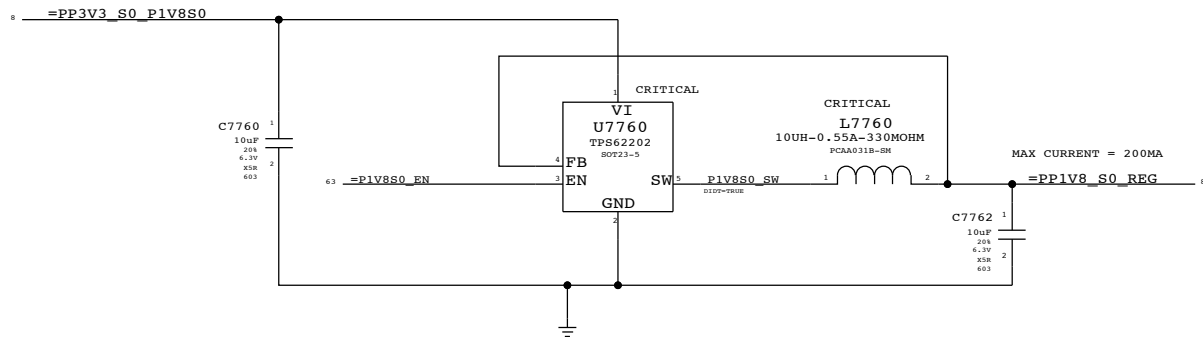
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CPUVTT POWER SUPPLY

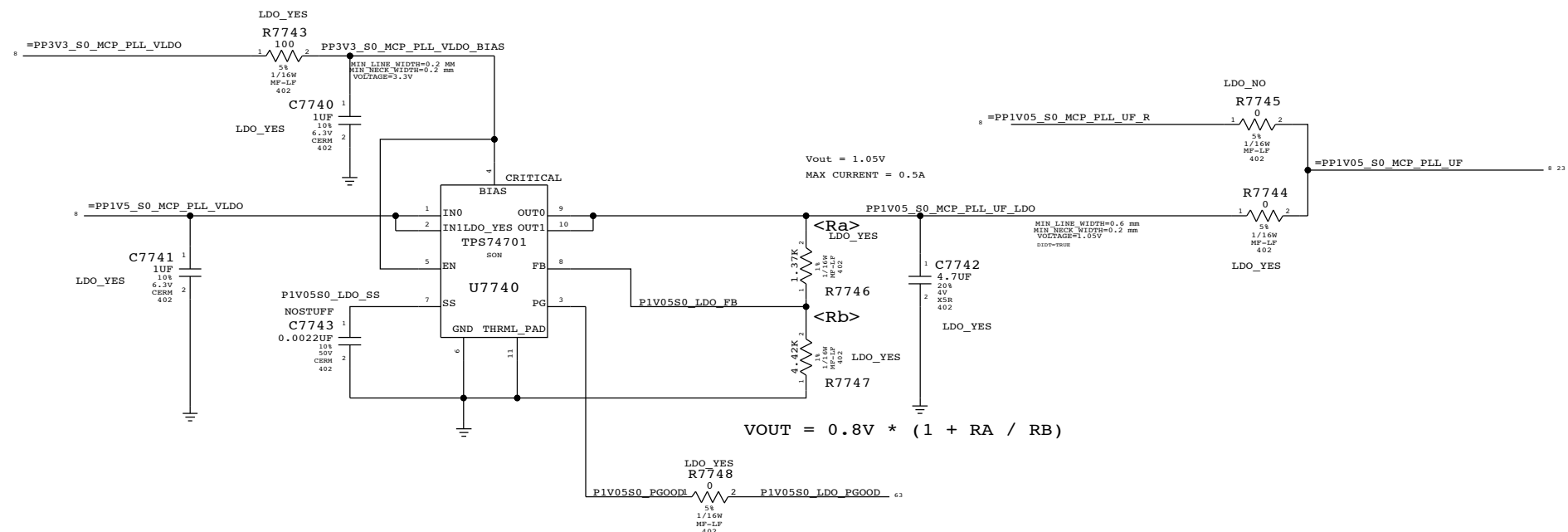


SYNC MASTER=K24 MLB		SYNC DATE=02/04/2009	
PAGE TITLE			
CPU VTT(1.05V)		SUPPLY	
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		14.5.0	
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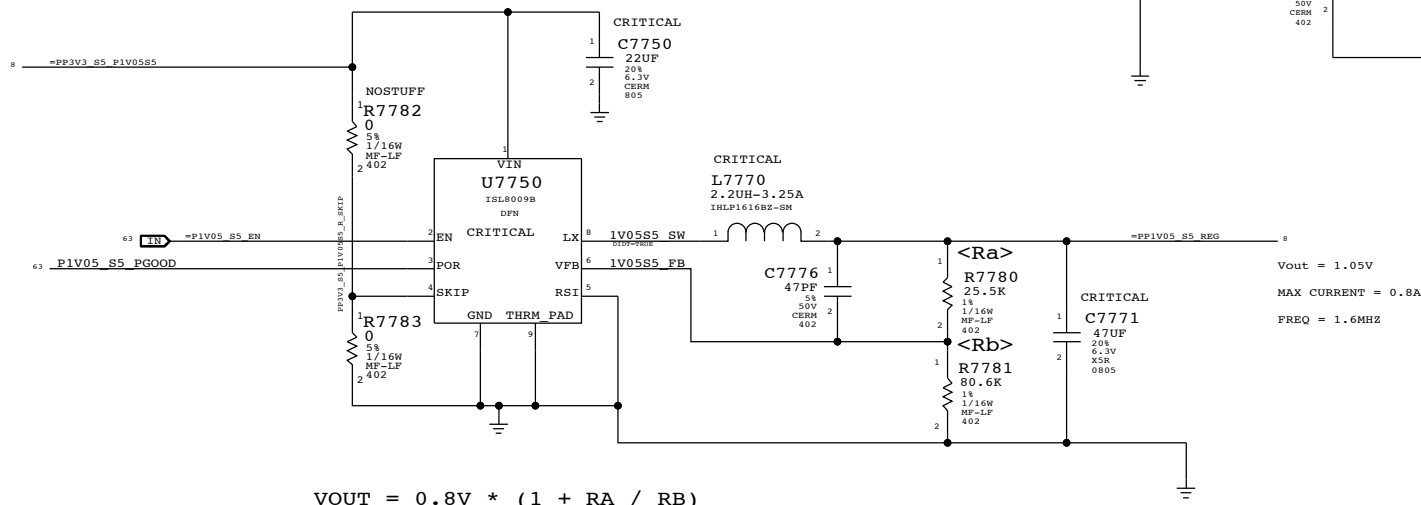
1.8V S0 SWITCHER



1.05V S0 PLL LDO

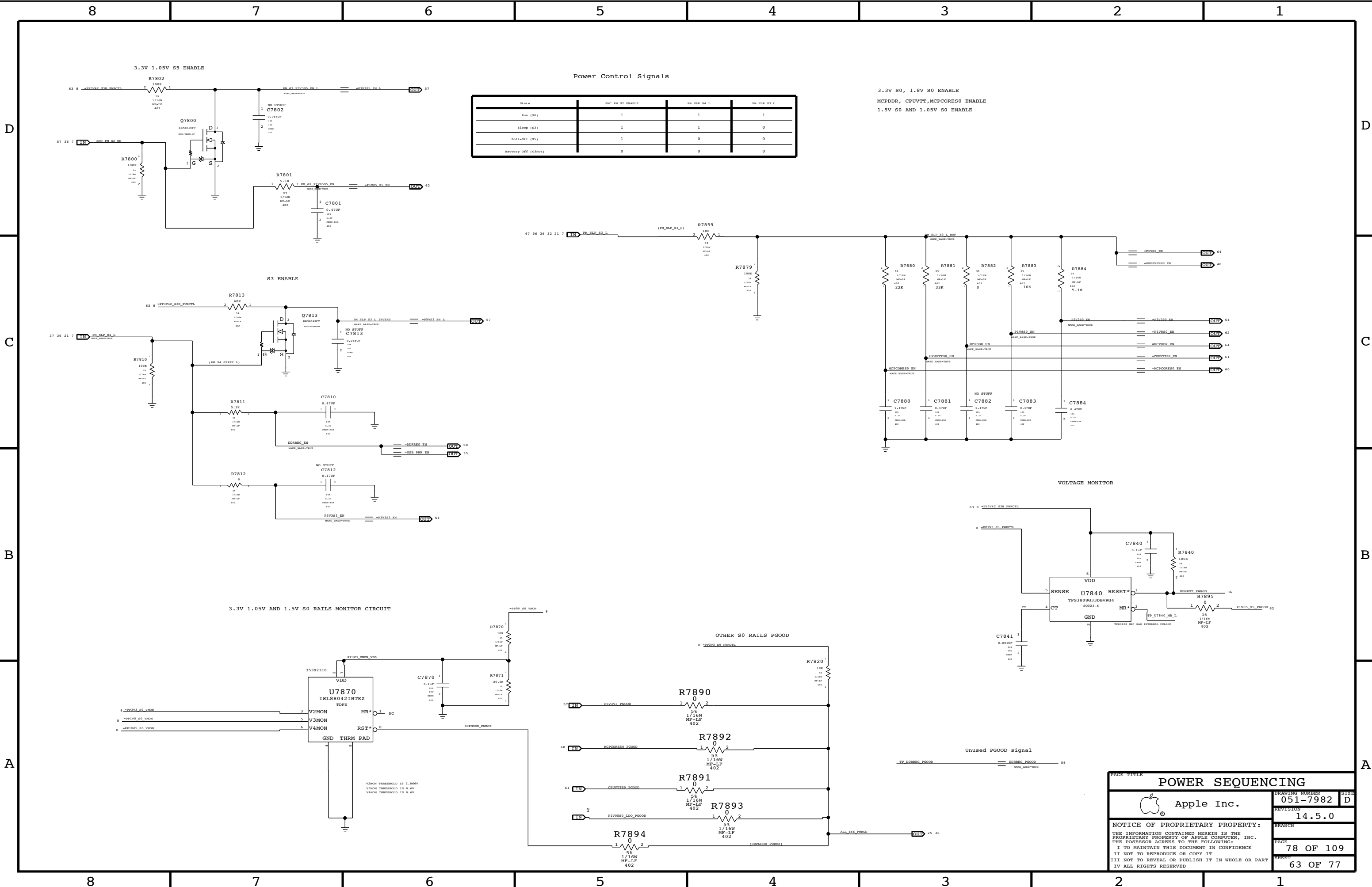


MCP 1.05V S5 (AUXC) SUPPLY



$$V_{OUT} = 0.8V * (1 + R_A / R_B)$$

SYNC MASTER=K24 MLB		SYNC DATE=03/24/2009	
PAGE TITLE			
MISC POWER SUPPLIES			
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Power Control Signals

State	SMC_PM_CU_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Bot)	0	0	0

3.3V_S0, 1.8V_S0 ENABLE
MCPDDR, CPUVTT,MCPCORES0 ENABLE
1.5V S0 AND 1.05V S0 ENABLE

VOLTAGE MONITOR

POWER SEQUENCING

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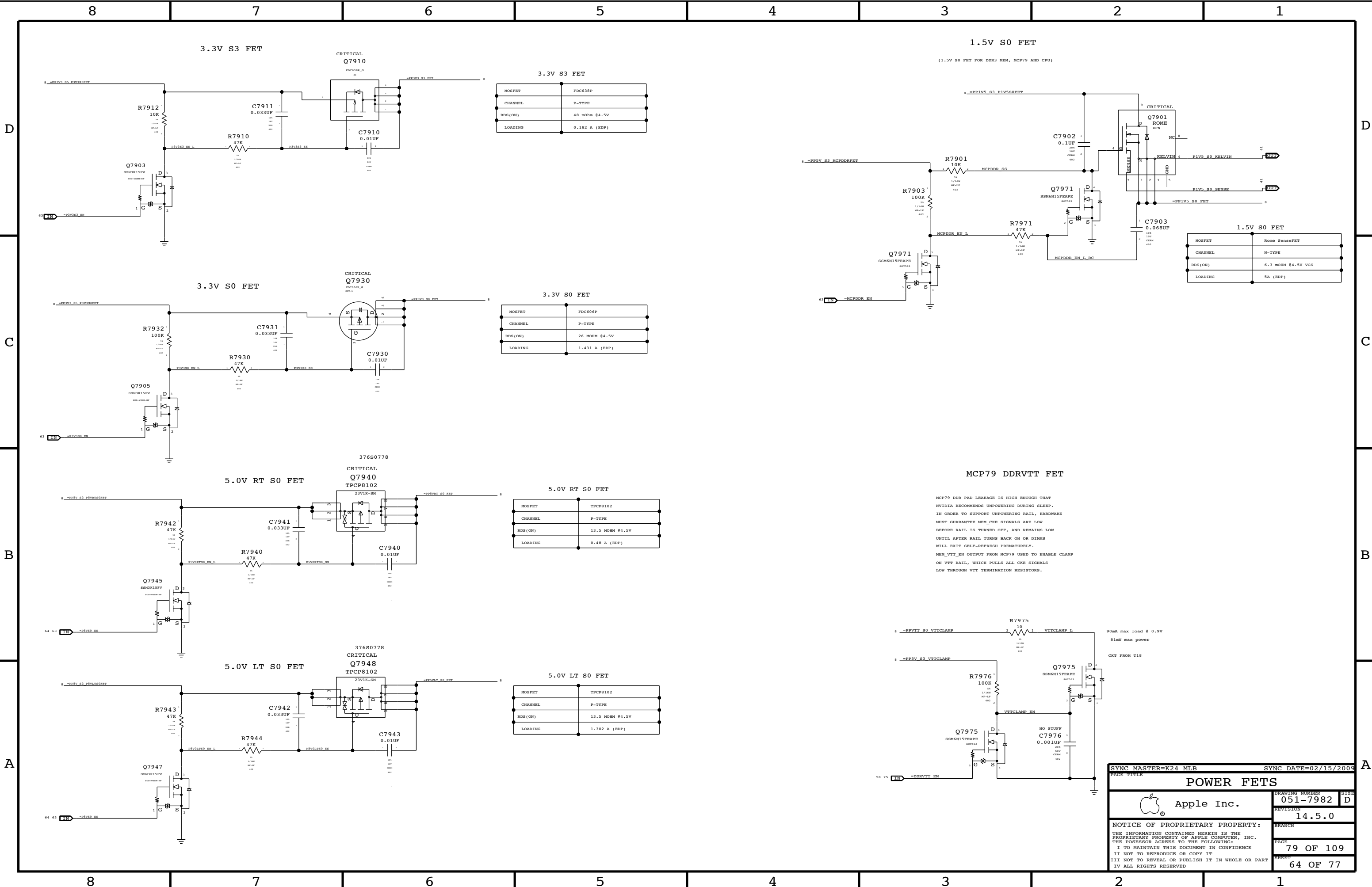
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SIZE
D



MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.

SYNC MASTER=K24 MLB

SYNC DATE=02/15/2009

POWER FETS

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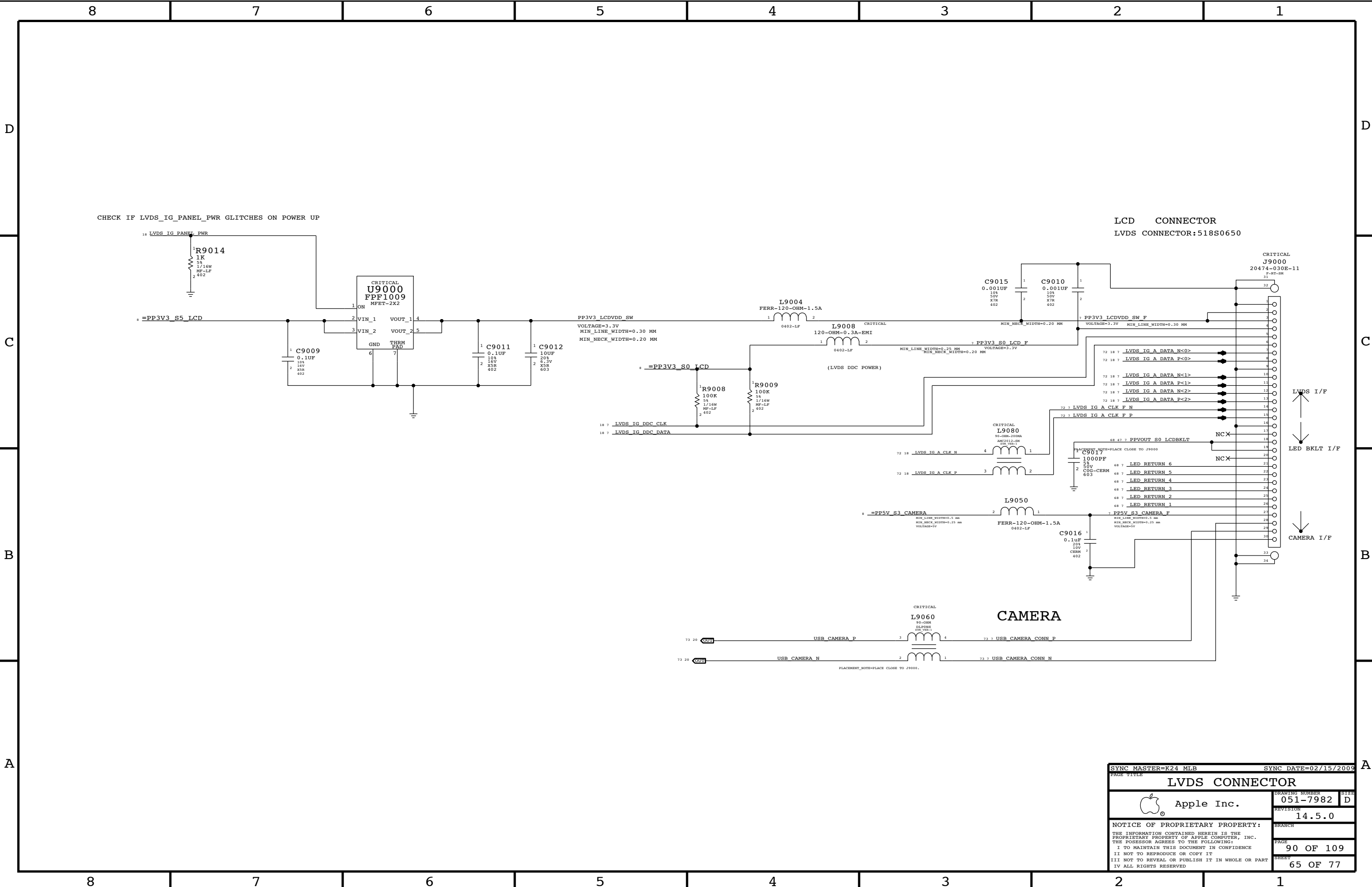
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LVDS CONNECTOR			
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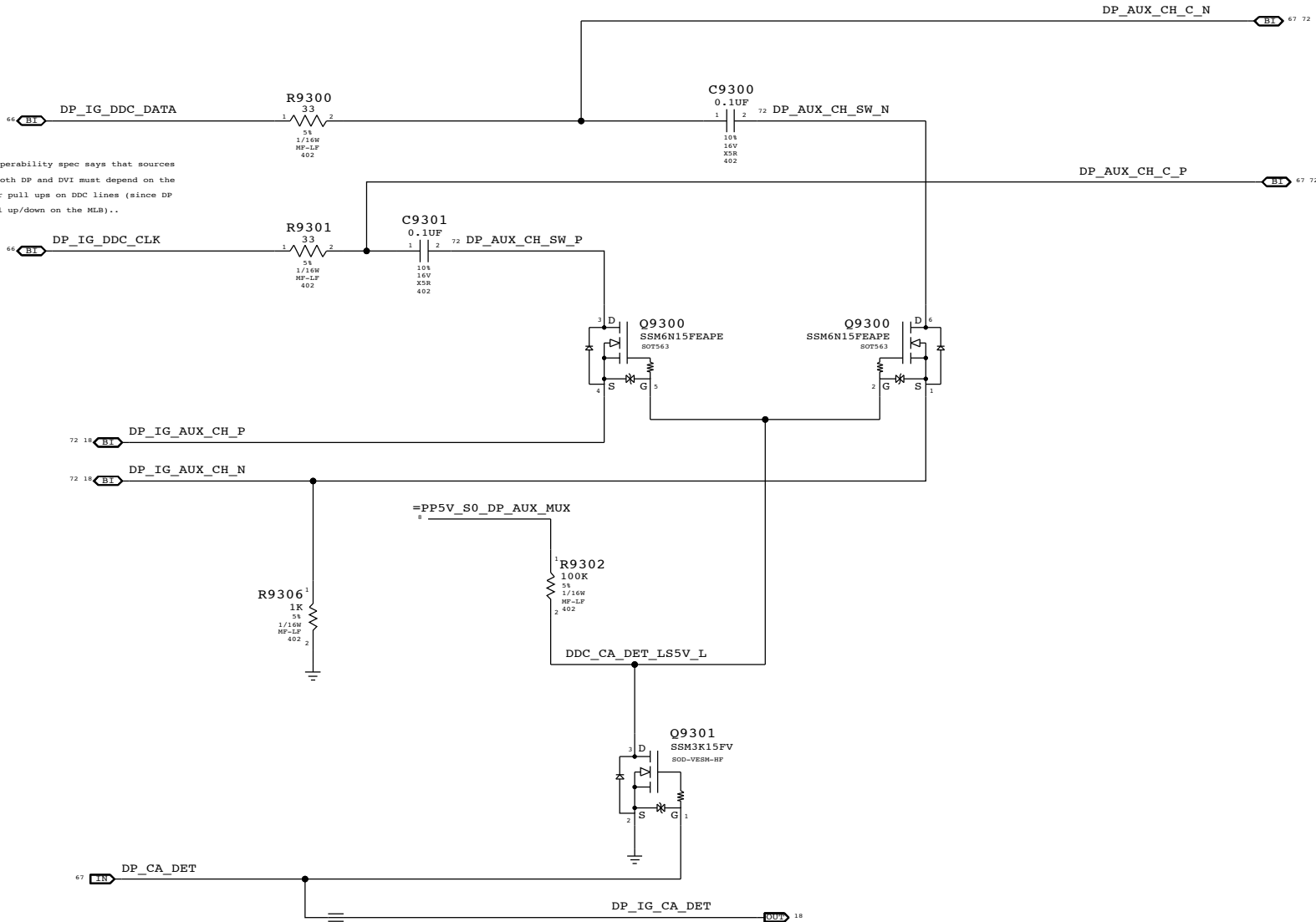
4

3

2

1

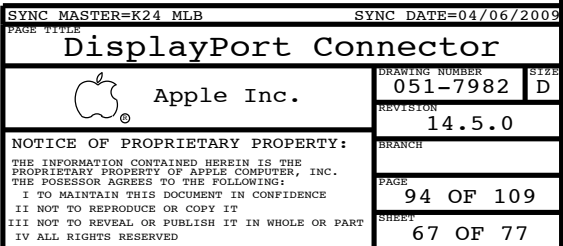
Display Port Interoperability spec says that sources or sinks which do both DP and DVI must depend on the external adapter for pull ups on DDC lines (since DP AUX CH has 100K pull up/down on the MLB)..



18	=MCP_HDMI_TXC_P	---	DP_ML_P<3>	---	67	72
18	=MCP_HDMI_TXC_N	---	DP_ML_N<3>	---	67	72
18	=MCP_HDMI_TXD_P<0>	---	DP_ML_P<2>	---	67	72
18	=MCP_HDMI_TXD_N<0>	---	DP_ML_N<2>	---	67	72
18	=MCP_HDMI_TXD_P<1>	---	DP_ML_P<1>	---	67	72
18	=MCP_HDMI_TXD_N<1>	---	DP_ML_N<1>	---	67	72
18	=MCP_HDMI_TXD_P<2>	---	DP_ML_P<0>	---	67	72
18	=MCP_HDMI_TXD_N<2>	---	DP_ML_N<0>	---	67	72
18	=MCP_HDMI_HPD	---	DP_HPD	---	67	
18	=MCP_HDMI_DDC_CLK	---	DP_IG_DDC_CLK	---	66	
18	=MCP_HDMI_DDC_DATA	---	DP_IG_DDC_DATA	---	66	

SYNC MASTER=K24 MLB		SYNC DATE=04/06/2009	
PAGE TITLE			
DISPLAYPORT SUPPORT			
 Apple Inc.		DRAWING NUMBER	051-7982
		REVISION	14.5.0
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Port Power Switch



D

C

B

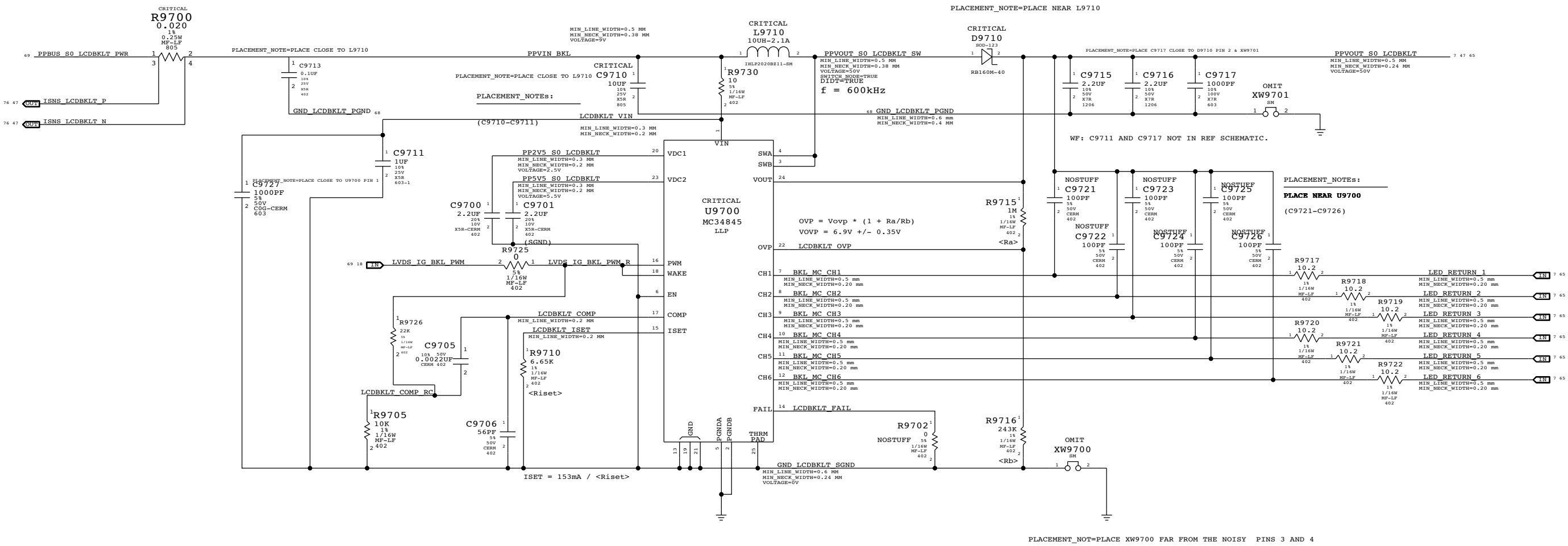
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A



13.3 Inch Panel (9 LEDs per string)
Target: ISET = 23mA, OVP = 35V
ACTUAL: ISET = 23mA, OVP = 35.2V

SYNC MASTER=VEMURI K19I		SYNC DATE=02/09/2009	
PAGE TITLE			
LCD Backlight Driver (MC34845)			
	DRAWING NUMBER		SIZE
	051-7982		D
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSD_DATA	*	=2x_DIELECTRIC	?	FSD_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSD_D0TB	*	=3x_DIELECTRIC	?	FSD_D0TB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSD_AD0R	*	=STANDARD	?	FSD_AD0R	TOP,BOTTOM	=3x_DIELECTRIC	?
FSD_AD0TB	*	=2x_DIELECTRIC	?	FSD_AD0TB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSD_1X	*	=STANDARD	?	FSD_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AOTL	*	=STANDARD	?
CPU_BMIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_OTLREF	*	25 MIL	?
CPU_ITP	*	=2:1 SPACING	?
CPU_VCCBENSE	*	25 MIL	?

SR DG recommends at least 25 mils, >50 mils preferred

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AOTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

ELECTRICAL_CONSTRAINT_SET		SST_TYPE			
		PHYSICAL	SPACING		
	FSS_DATA_GROUP0	FSS_S01	FSS_DATA1	FSSB D I<15..0>	10 14
	FSS_DATA_GROUP2	FSS_S02	FSS_DATA2	FSSB DINV I<0>	10 14
	FSS_DSTR0	FSS_DSTR0_S00	FSS_DSTR0	FSSB DSTR0_P<0>	10 14
	FSS_DSTR0	FSS_DSTR0_S00	FSS_DSTR0	FSSB DSTR0_N<0>	10 14
	FSS_DATA_GROUP1	FSS_S03	FSS_DATA3	FSSB D I<31..16>	10 14
	FSS_DATA_GROUP3	FSS_S04	FSS_DATA4	FSSB DINV I<1>	10 14
	FSS_DSTR1	FSS_DSTR1_S00	FSS_DSTR1	FSSB DSTR1_P<1>	10 14
	FSS_DSTR1	FSS_DSTR1_S00	FSS_DSTR1	FSSB DSTR1_N<1>	10 14
	FSS_DATA_GROUP2	FSS_S05	FSS_DATA5	FSSB D I<47..32>	10 14
	FSS_DATA_GROUP2	FSS_S05	FSS_DATA5	FSSB DINV I<2>	10 14
	FSS_DSTR2	FSS_DSTR2_S00	FSS_DSTR2	FSSB DSTR2_P<2>	10 14
	FSS_DSTR2	FSS_DSTR2_S00	FSS_DSTR2	FSSB DSTR2_N<2>	10 14
	FSS_DATA_GROUP3	FSS_S06	FSS_DATA6	FSSB D I<63..48>	10 14
	FSS_DATA_GROUP3	FSS_S06	FSS_DATA6	FSSB DINV I<3>	10 14
	FSS_DSTR3	FSS_DSTR3_S00	FSS_DSTR3	FSSB DSTR3_P<3>	10 14
	FSS_DSTR3	FSS_DSTR3_S00	FSS_DSTR3	FSSB DSTR3_N<3>	10 14
	FSS_ADDR_GROUP0	FSS_S07	FSS_ADDR0	FSSB A I<16..3>	10 14
	FSS_ADDR_GROUP0	FSS_S07	FSS_ADDR0	FSSB REW I<4..0>	10 14
	FSS_ADDR0	FSS_ADDR0_S00	FSS_ADDR0	FSSB ADSTRB I<0>	10 14
	FSS_ADDR_GROUP1	FSS_S08	FSS_ADDR1	FSSB A I<35..17>	10 14
	FSS_ADDR0	FSS_ADDR0_S00	FSS_ADDR0	FSSB ADSTRB I<1>	10 14
	FSS_LX	FSS_S09	FSS_LX1	FSSB ADS L	10 14
	FSS_BREQ0_L	FSS_S09	FSS_LX1	FSSB BREQ0 L	10 14
	FSS_BREQ0_L	FSS_S09	FSS_LX1	FSSB BREQ0 I	14
	FSS_LX	FSS_S09	FSS_LX1	FSSB BNR L	10 14
	FSS_LX	FSS_S09	FSS_LX1	FSSB BERR L	10 14
	FSS_LX	FSS_S09	FSS_LX1	FSSB DBSY L	10 14
	FSS_LX	FSS_S09	FSS_LX1	FSSB DEFERR L	10 14
	FSS_LX	FSS_S09	FSS_LX1	FSSB ORDY L	10 14
	FSS_LX	FSS_S09	FSS_LX1	FSSB HIT L	10 14
	FSS_LX	FSS_S09	FSS_LX1	FSSB HITM L	10 14
	FSS_LX	FSS_S09	FSS_LX1	FSSB LOCK L	10 14
	FSS_CPUREST_L	FSS_S09	FSS_LX1	FSSB CPUREST L	10 13 14
	FSS_LX	FSS_S09	FSS_LX1	FSSB RS I<2..0>	10 14
	FSS_LX	FSS_S09	FSS_LX1	FSSB TRDY L	10 14
	CPU_A2GM	CPU_S00	CPU_B001	CPU A2GM L	10 14
	CPU_BERR	CPU_S00	CPU_B001	CPU BERR<2..0>	9 10
	CPU_FERR_L	CPU_S00	CPU_B011	CPU FERR L	10 14
	CPU_IGNNE_L	CPU_S00	CPU_B001	CPU IGNNE L	10 14
	CPU_INIT_L	CPU_S00	CPU_B001	CPU INIT L	10 14
	CPU_ISTRM_L	CPU_S00	CPU_B001	CPU INTR	10 14
	CPU_ISTRM_L	CPU_S00	CPU_B001	CPU NMI	10 14
	CPU_PROCHOT_L	CPU_S00	CPU_B001	CPU PROCHOT L	14 37
	CPU_PWDG0	CPU_S00	CPU_B001	CPU PWDG0	10 13 14
	CPU_ISTRM_L	CPU_S00	CPU_B001	CPU RMI L	10 14
	CPU_ISTRM_L	CPU_S00	CPU_B001	CPU STECLK L	10 14
	PM_THERMTRIP_L	CPU_S00	CPU_B011	PM THERMTRIP L	14 37
	FSS_CPUREST_L	CPU_S00	CPU_B001	FSSB CPUREST L	10 14
	CPU_DPSEL_P0	CPU_S00	CPU_B001	CPU DPSEL L	10 14
	CPU_DPSEL_P1	CPU_S00	CPU_B001	CPU DPSEL L	10 59
	CPU_ISTRM_L	CPU_S00	CPU_B001	FSSB DPWR L	10 14
	MCP_CPU_COMP	MCP_S00	MCP_F001_COMP	MCP BCLK VML COMP VDD	14
	MCP_CPU_COMP	MCP_S00	MCP_F001_COMP	MCP BCLK VML COMP GND	14
	MCP_CPU_COMP	MCP_S00	MCP_F001_COMP	MCP CPU COMP VCC	14
	MCP_CPU_COMP	MCP_S00	MCP_F001_COMP	MCP CPU COMP GND	14
	FSS_CLK_CPU	CLK_F001_1000	CLK_F001	FSSB CLK CPU P	10 14
	FSS_CLK_CPU	CLK_F001_1000	CLK_F001	FSSB CLK CPU N	10 14
	FSS_CLK_ITP	CLK_F001_1000	CLK_F001	FSSB CLK ITP P	13 14
	FSS_CLK_ITP	CLK_F001_1000	CLK_F001	FSSB CLK ITP N	13 14
	FSS_CLK_MCP	CLK_F001_1000	CLK_F001	FSSB CLK MCP P	14
	FSS_CLK_MCP	CLK_F001_1000	CLK_F001	FSSB CLK MCP N	14
	CPU_IERR_L	CPU_S00		CPU IERR L	10
	PM_DPSEL_P0	CPU_S00	CPU_B001	PM DPSEL_P0	21 59
	(See above)	CPU_S00	CPU_B001	IMVP DPSEL_P0	59
	CPU_OTLREF	CPU_S00	CPU_OTLREF	CPU OTLREF	10 26
	CPU_COMP	CPU_S00	CPU_COMP	CPU COMP<3>	10
	CPU_COMP	CPU_120A0	CPU_COMP	CPU COMP<2>	10
	CPU_COMP	CPU_S00	CPU_COMP	CPU COMP<1>	10
	CPU_COMP	CPU_120A0	CPU_COMP	CPU COMP<0>	

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLX_PCIE	*	20 MIL	?
NCP_FEX_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_10G0	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_10G0	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
NCP_OV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP97 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OBM_DIFF	=100_OBM_DIFF	=100_OBM_DIFF	=100_OBM_DIFF	=100_OBM_DIFF	=100_OBM_DIFF
SATA_90D_HD0	*	=90_OBM_DIFF	=90_OBM_DIFF	=90_OBM_DIFF	=90_OBM_DIFF	=90_OBM_DIFF	=90_OBM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4X_DIELECTRIC	?
SATA_TERM	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL CONSTRAINT SET		NET_TYPE			
		PHYSICAL	SPACING		
		PCIE_800	PCIE	PCIE MINI R2D P	30
		PCIE_800	PCIE	PCIE MINI R2D N	30
	PCIE_MINI_R2D	PCIE_800	PCIE	PCIE MINI R2D C P	17 30
		PCIE_800	PCIE	PCIE MINI R2D C N	17 30
	PCIE_MINI_D2R	PCIE_800	PCIE	PCIE MINI D2R P	17 30
		PCIE_800	PCIE	PCIE MINI D2R N	17 30
		PCIE_800	PCIE	PCIE FW R2D P	
		PCIE_800	PCIE	PCIE FW R2D N	
	PCIE_FW_R2D	PCIE_800	PCIE	PCIE FW R2D C P	9 17
		PCIE_800	PCIE	PCIE FW R2D C N	9 17
	PCIE_FW_D2R	PCIE_800	PCIE	PCIE FW D2R P	9 17
		PCIE_800	PCIE	PCIE FW D2R N	9 17
		PCIE_800	PCIE	PCIE FW D2R C P	
		PCIE_800	PCIE	PCIE FW D2R C N	
	MCP_CLK100M	CLK_PCIE_1000	CLK_PCIE	PCIE CLK100M MINI P	17 30
		CLK_PCIE_1000	CLK_PCIE	PCIE CLK100M MINI N	17 30
		CLK_PCIE_1000	CLK_PCIE	PCIE CLK100M MINI CONN P	7 30
		CLK_PCIE_1000	CLK_PCIE	PCIE CLK100M MINI CONN N	7 30
	MCP_CLK100M_FC	CLK_PCIE_1000	CLK_PCIE	PCIE CLK100M FC P	
		CLK_PCIE_1000	CLK_PCIE	PCIE CLK100M FC N	
		PCIE_800	PCIE	CONN PCIE MINI R2D P	7 30
		PCIE_800	PCIE	CONN PCIE MINI R2D N	7 30
		PCIE_800	PCIE	CONN PCIE MINI D2R P	7 30
		PCIE_800	PCIE	CONN PCIE MINI D2R N	7 30
	MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP PEX CLK COMP	17
	TMDS_IG_TXC	DP_1000	DISPLAYPORT	TMDS IG TXC P	
	TMDS_IG_TXC	DP_1000	DISPLAYPORT	TMDS IG TXC N	
	TMDS_IG_TXD	DP_1000	DISPLAYPORT	TMDS IG TXD P<2,,0>	
	TMDS_IG_TXD	DP_1000	DISPLAYPORT	TMDS IG TXD N<2,,0>	
	DP_ML	DP_1000	DISPLAYPORT	DP ML P<3,,0>	66 67
	DP_ML	DP_1000	DISPLAYPORT	DP ML C P<3,,0>	66 67
	DP_ML	DP_1000	DISPLAYPORT	DP ML N<3,,0>	67
	DP_ML	DP_1000	DISPLAYPORT	DP ML C N<3,,0>	67
	DP_AUX_CH	DP_1000	DISPLAYPORT	DP IG AUX CH P	18 66
	DP_AUX_CH	DP_1000	DISPLAYPORT	DP IG AUX CH N	18 66
	DP_AUX_CH	DP_1000	DISPLAYPORT	DP AUX CH SW P	66
	DP_AUX_CH	DP_1000	DISPLAYPORT	DP AUX CH SW N	66
	DP_AUX_CH	DP_1000	DISPLAYPORT	DP AUX CH C P	66 67
	DP_AUX_CH	DP_1000	DISPLAYPORT	DP AUX CH C N	66 67
	MCP_HDMI_RSET	MCP_HV_COMP		MCP HDMI RSET	18 24
	MCP_HDMI_VPROBE	MCP_HV_COMP		MCP HDMI VPROBE	18 24
	LVDS_IG_A_CLK	LVDS_1000	LVDS	LVDS IG A CLK P	18 65
	LVDS_IG_A_CLK	LVDS_1000	LVDS	LVDS IG A CLK F P	7 65
	LVDS_IG_A_CLK	LVDS_1000	LVDS	LVDS IG A CLK N	18 65
	LVDS_IG_A_CLK	LVDS_1000	LVDS	LVDS IG A CLK F N	7 65
	LVDS_IG_A_DATA	LVDS_1000	LVDS	LVDS IG A DATA P<2,,0>	7 18 65
	LVDS_IG_A_DATA	LVDS_1000	LVDS	LVDS IG A DATA N<2,,0>	7 18 65
	DP_ML	DP_1000	DISPLAYPORT	DP ML CONN P<3,,0>	67
	DP_ML	DP_1000	DISPLAYPORT	DP ML CONN N<3,,0>	67
	MCP_IPFAB_RSET	MCP_HV_COMP		MCP IPFAB RSET	18 24
	MCP_IPFAB_VPROBE	MCP_HV_COMP		MCP IPFAB VPROBE	18 24
	SATA_HDD_R2D	SATA_800_HDD	SATA	SATA HDD R2D C P	20 34
	SATA_HDD_R2D	SATA_800_HDD	SATA	SATA HDD R2D C N	20 34
	SATA_HDD_R2D	SATA_800_HDD	SATA	SATA HDD R2D P	7 34
	SATA_HDD_R2D	SATA_800_HDD	SATA	SATA HDD R2D N	7 34
	SATA_HDD_R2D	SATA_800_HDD	SATA	SATA HDD R2D UF P	34
	SATA_HDD_R2D	SATA_800_HDD	SATA	SATA HDD R2D UF N	34
	SATA_HDD_D2R	SATA_800_HDD	SATA	SATA HDD D2R P	20 34
	SATA_HDD_D2R	SATA_800_HDD	SATA	SATA HDD D2R N	20 34
	SATA_HDD_D2R	SATA_800_HDD	SATA	SATA HDD D2R C P	7 34
	SATA_HDD_D2R	SATA_800_HDD	SATA	SATA HDD D2R C N	7 34
	SATA_HDD_D2R	SATA_800_HDD	SATA	SATA HDD D2R UF P	34
	SATA_HDD_D2R	SATA_800_HDD	SATA	SATA HDD D2R UF N	34
	SATA_ODD_R2D	SATA_1000	SATA	SATA ODD R2D C P	20 34
	SATA_ODD_R2D	SATA_1000	SATA	SATA ODD R2D C N	20 34
	SATA_ODD_R2D	SATA_1000	SATA	SATA ODD R2D P	7 34
	SATA_ODD_R2D	SATA_1000	SATA	SATA ODD R2D N	7 34
	SATA_ODD_R2D	SATA_1000	SATA	SATA ODD R2D UF P	34
	SATA_ODD_R2D	SATA_1000	SATA	SATA ODD R2D UF N	34
	SATA_ODD_D2R	SATA_1000	SATA	SATA ODD D2R P	20 34
	SATA_ODD_D2R	SATA_1000	SATA	SATA ODD D2R N	20 34
	SATA_ODD_D2R	SATA_1000	SATA	SATA ODD D2R C P	7 34
	SATA_ODD_D2R	SATA_1000	SATA	SATA ODD D2R C N	7 34
	SATA_ODD_D2R	SATA_1000	SATA	SATA ODD D2R UF P	34
	SATA_ODD_D2R	SATA_1000	SATA	SATA ODD D2R UF N	34
	MCP_SATA_TERM		SATA_TERM	MCP SATA_TERM	20

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